As demand increases for advanced PCBAs across a wide range of industries, so has the need for innovative manufacturing solutions that enable the next generation of SMT production. The emergence of electric vehicles, bio-medical monitoring and increasing speed and bandwidth requirements for telecommunications infrastructure, are all contributing to the need for advanced PCB designs.

Over the past decade, the growing complexity of PCBAs has become evident [1]. Pin counts have more than doubled, with as many as 4,200 terminations. Minimum termination pitches of 16 mils have become commonplace, with some high value production today having a pitch of 12 mils. Electronic Manufacturing Services (EMS) companies and OEM’s continually work to define design rules that support higher performance requirements, while still being manufacturable.

For automotive applications, engineers at EMS companies have developed expertise in material selection and processing to manage high power and high voltage devices in electric and hybrid vehicles. These materials optimize thermal conductivity while simultaneously providing isolation for high power. The Internet of Things and bio-medical monitoring have driven the need for smaller connected sensors. These sensors require very high levels of reliability and sensitivity, necessitating the selection of new materials and higher levels of cleanliness.

Another driver is speed, increasing power and mixed signal integration with power and ground pins for different power domains. Also, PCB designers want passive components as close to a chip’s power and ground pins as possible to improve decoupling. PCB technology is being driven to minimize chip-to-chip spacing in order to increase speed and signal integrity. Increasing performance at a lower cost drives demand for bottom terminated components (BTC). Designs with tighter chip and component spacing, however, present challenges if rework is required.

Some of the key technology challenges OEMs and EMS providers have been working to solve include: selection and processing of specialized materials, cleaning PCBAs, minimizing voids in BTCs, reducing the pitch between components while retaining sufficient space for rework, eliminating head-on-pillow defects in connections and building PCBAs for mission critical applications. These issues continue to drive extraordinary advances in SMT processes as the number of terminations increase and pad pitch decreases. Some of the latest SMT technology challenges currently being addressed include:

**HIGH POWER DEVICES REQUIRE EXPERTISE WITH UNIQUE MATERIALS**

High power applications common in hybrid cars, electric automobiles and high-power LED lighting require specialist materials expertise to select and process substances used in manufacturing. Power management integrated circuits (ICs) are used in inverters, converters, chargers and powertrain systems. Typically, high power applications require 1,000 to 4,000 volts and these high voltages give rise to die temperatures approaching 170°C in some devices. It is critical to have good thermal conductivity between the device and the PCB to transfer the heat efficiently and to allow it to dissipate through heat sinks. However, because of the very high voltages, good insulation is also required. The characteristics of the material chosen to connect high power devices to a PCB must include good thermal conductivity and good dielectric properties. Automotive applications present the most pronounced challenge. Unique components on the leading edge of technology used in some applications require expertise in selecting the most suitable material to optimize thermal conductivity, dielectric properties as well as manufacturability. Dispensing, processing and curing these materials during the manufacturing process present additional challenges. For example, materials with both good thermal conductivity and insulation properties often have abrasive characteristics. When the material is pushed through dispensing equipment, it can reduce equipment lifetime. More importantly, air trapped during the dispensing process can create an arcing problem in the high power device. Vacuum mixing methods have been developed to dispense the material in a uniform layer and eliminate the possibility of trapped air.

**VERY SMALL LEAKAGE CURRENTS PRESENT CLEANING CHALLENGES**

Advanced electronic designs in telecommunications, automotive and medical applications require PCBs having extremely small leakage currents. Sensors worn on the human body, high speed telecommunications and high power automotive applications require very high levels of insulation. Today’s leading edge designs require insulation levels measured in tera ohms (10^{12} ohms), whereas insulations of 10^{8} ohms were sufficient several years ago.

No-clean fluxes used in most SMT assembly processes leave weak organic acid (WOA) residues. These residues can reduce surface insulation levels. As a result, the cleaning and measurement of cleanliness on PCBAs has become a critical process requiring high precision and repeatability.

Components with stand-off height from the substrate as low as 2 mils pose a technical challenge for cleaning. With this very low profile, it is difficult to expel the water from under the device. Solutions have been developed using a Saniflow to reduce the surface tension of the water and allow it to flow out from under devices with very low profiles. However, maintaining an optimal concentration of the chemical for effective cleaning while reducing its adverse effect continues to be a critical challenge.

There are a number of methods used to measure PCB cleanliness. Ion chromatography is used to find and quantify anions, cations and WOAs. It measures ion concentration on the PCB after cleaning. Surface Insulation Resistance (SIR) measures the resistivity on the surface of the PCB. Typically, SIR is continually monitored over a period of seven days, while humidity is maintained at 85 percent. Both of these measurement methods are complementary and are used as part of qualification and validation to verify that the SMT production process is capable of achieving the high levels of cleanliness and surface insulation resistance required.

**REDUCING VOIDING IN BTCs**

PCBs with BTCs are increasingly common, as BTCs have the advantage of offering good performance—both in signal integrity and thermal performance— at a relatively low cost. However, increasing pin count, package size and reduced pitch on BTCs creates production challenges. The increased pin count allows more functionality and manufacturing faces new challenges in producing reliable contacts with these large-surface-area devices. The biggest challenge with BTC packages is thermal pad voiding. During the solder reflow process, chemicals or air can be trapped in the solder, creating voids that may impact thermal conductivity or solder joint reliability. BTCs are used for very high speed switching. The devices can increase in temperature very quickly. Large voids restrict heat dissipation, causing an increase in temperature to the point where transient failures can occur. Thermal pads present a unique challenge during reflow, as the pads are typically larger and connected to large copper areas within the PCB. Therefore, they require proper solder volume control and optimized reflow profiles to ensure adequate solder coverage with minimum voiding. Stencil
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in volume production.

Rework Challenges Rise as Components Spacing Decreases

OEMs are focused on functionality and performance. The use of decoupling capacitors for noise reduction leads to designs with more interconnects and smaller components. New designs, with more demanding signal integrity requirements, can result in conflicts between layout requirements and what can be manufactured. With the conflicts between design requirements and process capability, rework is becoming a challenge. For some high performance computing and communications PCBAs produced at Sanmina, the cost of a single PCB can be over $15,000. Therefore, it is imperative that the assembly is not damaged during rework. Furthermore, adequate spacing between components is also required to ensure that heat used for rework does not damage the solder joints of adjacent components, or the components themselves. While IPC standards do not provide strict requirements for component spacing, and current SMT assembly processes can accommodate tight spacing, experience has shown that at least 100 mils of space should be left around large ball-grid arrays to allow for rework. This is a major reduction from the 200 mils clearance requirements of five years ago. OEMs are now pushing decoupling capacitors as close as 17 mils in order to optimize noise performance. Because some components lose functional performance when exposed to temperatures exceeding 120°C, tighter spacing constrains the ability to perform rework. Complex and sophisticated thermal isolation schemes have been developed for these applications, but this rework technology is costly. EMS companies are working with equipment manufacturers to develop processes, robotic soldering solutions, cleaning systems and rework tooling that make reliable, repeatable rework possible, without inducing secondary reflow or additional rework of adjacent components. Although current solutions exist for keep-out space values well below 100 mils, additional process development and tooling enhancements are necessary to accommodate repair with tighter component spacings.

In addition to the mechanics of soldering and navigating rework equipment in the confines of tight dimensions, metallurgy is an important aspect of repair. In the Tin-Silver-Copper solder alloy system, repair can potentially introduce voiding. Vacuum reflow has also been developed as a solution and is now used in volume production.

Chip Package Warpage

To minimize cost, ICs are often mounted in plastic packages. However, plastic is thermally less stable than ceramic. When plastic packages are exposed to high temperatures during reflow, the package can warp 2-10 mils more or less, depending on the substrate, plastic material properties, die size, package thickness and package size. A combination of package and PCB substrate dynamic warpage, along with PCB pad solderability issues and variations in printed solder paste volume, can result in solder defects between a device and the PCB. Two common defects are head-on-pillow (HOP), or non-wet open (NWO) type defects. While NWO defects create solder joints with no electrical continuity, HOP defects can be partially opened with intermittent connections. Current screening methods for HOP defects involve expensive 3D X-Ray inspection. However, this method is not advanced enough to be 100 percent effective. It is also time-consuming and resource-intensive. The best solution to the HOP issue is prevention by adopting a tighter specification for warpage.

The JEDEC specification for package warpage, revised in 2001, allows for a maximum of 8 mils of co-planarity at room temperature. Component suppliers usually provide specifications for room temperature co-planarity, using either the seating plane or the PCB pad. As long as the value is under 8 mils, the co-planarity is deemed within specification. Empirical data suggests that the JEDEC specification is no longer adequate [3]. For high pin count packages with small pad areas and lower solder volumes, production data suggests that component warpage exceeding 3.5 mils can cause problems during reflow, with a high potential for HOP defects. Manufacturers of consumer devices may discard or recycle defective boards, but this is not an option for an advanced computing or communications PCB costing over $20,000. EMS providers will continue to drive changes to improve PCB co-planarity. As the JEDEC specification for package warpage is not an option for an advanced computing or communications industry, the JEDEC specification for package warpage of 3.5 mils for high pin count devices will need to be pushed to 10 mils or more.

Building PCBAs for Mission Critical Environments

Industries such as oil and gas use electronic assemblies in very demanding environments. Drilling and exploration tools used two to three miles below the earth’s surface can cost upwards of $2 million and operate in environments with temperatures up to 170°C at 50 Atm pressure. The solder material used in these assemblies

requires temperatures above 290°C in order to reflow. In the absence of mass reflow options for high melting temperature solder alloys, hand soldering has become the only alternative for such applications.

The medical, automotive and aerospace industries are highly regulated. Advanced technology designed into electronic systems used in these industries requires sophisticated SMT manufacturing techniques. However, the manufacturing process used must also comply with stringent regulatory requirements. Regulatory compliance typically requires some form of validation and assurance, whether it’s a validation of each PCB produced according to the design and manufacturing process specifications.

Looking Ahead

Advanced PCBAs driven by superior signal integrity, miniaturization, higher densities and increasing I/O counts will continue to push the competing technical boundaries in SMT production. High power applications in high density SMT package requirements for lower leakage current will continue to pose new manufacturing challenges. This will lead to the development of new technology, including automation and special handling solutions. New expertise in the selection and processing of chemicals and polymers to achieve isolation and conductivity goals will also be essential. The environment in which SMT production takes place will become increasingly important. Vacuum reflow is now standard in volume production and it is likely that going forward, more and more high density SMT assembly will have to be done in clean rooms.

References:


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