IMPACT OF MICROVIA-IN-PAD DESIGN ON VOID FORMATION

Frank Grano, Felix Bruno
Huntsville, AL

Dana Korf, Eamon O'Keeffe
San Jose, CA

Cheryl Kelley
Salem, NH

Joint Paper by Sanmina-SCI Corporation EMS, GTS and PCB Divisions

ABSTRACT

Micro-vias are minute holes in circuit boards with a diameter of 6 mils or less that are placed within or underneath component pads. These structures allow the interconnection of outer and inner layers, which results in an increased routing area or available space for the placement of denser components. A via-in-pad is a plated-through hole that is used as an interlayer connection from a component land, but in which there is no intention to insert a component lead or other reinforcing material. However, the ability to either place vias on or off the pads gives designers greater flexibility to selectively create routing room in denser parts of the substrate.

This is phase 1 of an R&D project and this paper presents the solderability results for different via-in-pad locations and sizes based on assembly criteria. Although the design includes Ball Grid Arrays (BGAs), Quad Flat Packs (QFPs) and passive components, only BGAs were examined at this stage. Since the primary analysis will be void formation the samples were analyzed using X-Ray Laminography and conclusions drawn. The results of this experiment may not reflect the impact on high volume manufacturing.

BACKGROUND

The tendency in electronic devices is toward smaller and lighter devices with an increase in functionality. The size of products, such as cellular phones and camcorders, is a fraction of the size they were before. The improved product functionality comes next to the dramatic reduction in the size of the silicon packages and the Printed Circuit Boards (PCBs) [1].

Newer components such as Ball Grid Arrays (BGAs), Chip Scales Packages (CSPs) and Direct Chip Attach (DCA) devices have challenged the ability of technology associated with PCBs to manufacture cost effective boards. This is predominantly due to the higher number of I/Os (as high as 2500 I/Os) and the tighter pitches (as low as 0.5 mm) associated with these components compared to peripheral leaded devices. The increases in the number of I/Os require PCBs to allow signal distribution from these packages to the rest of the board. Different solutions have been proposed, such as fabrication of fine line circuitries and a reduction in the spaces between the lines. However, micro-via technology is one solution to the challenges imposed by the miniaturization of components utilized in current electronic assemblies. Micro-vias are the structures that allow the interconnection between different layers of the circuit board and thereby enhance the routing area for the connection of denser components [2].

Micro-vias are defined by IPC-2315 and IPC-6012A standards, as blind and buried vias that are equal to or less than 6 mils (152 microns) in diameter and have a target pad equal to or less than 14 mils (356 microns). The target pad is defined as the land on which a micro-via ends and makes a connection [3]. The micro-vias are placed on the substrate pads, namely via-in-pad, and are used to interconnect the different outer and inner layers of a PCB. The use of micro-via technology, coupled with the reduction of geometries of a conventional multilayered PCB, is termed as a High Density Interconnection (HDI) structure [4]. Typically, these structures use a traditional FR-4 core with build-up dielectric layers such as Resin Coated Copper (RCC).

Some of the reported advantages of the use of micro-vias are listed below [4]:

- They require smaller pad sizes, which save space in the PCB;
- Increase the wiring density in conventional FR-4 by a factor of 4;
- Reduce layer counts (33% of conventional boards);
- More chips can be placed on the PCB or a smaller PCB can be fabricated;
- In some cases, micro-vias improve the electrical performance due to the smaller via lengths and diameters and shorter pathways in comparison to the through hole; they reduce the cross talk and switching noises;

- Support surface mount components and DCA devices;
- Provide for better reliability in comparison to through hole vias due to lowest aspect ratio. A typical aspect ratio for through holes is 4 - 8 and for micro-vias is between 0.5 – 0.7; and
- Can be fabricated in rigid, flex or rigid/flex substrates.

EXPERIMENT

The main focus of this project is to determine the optimum design criteria when incorporating via-in-pad technology in a board design. The goal was to accomplish this by varying both the via-hole size and the location of the via-hole in the pad along with assembling these on a standard Surface Mount Technology (SMT) line. The data generated from this would then be given to the Sanmina-SCI PCB design group.

With this in mind a test-vehicle PCB was designed for this evaluation that was 8 layers with dimensions of 6.5" X 10". The use of 8 layers allowed the designers to best simulate the via-hole configurations currently being used. Dummy inner layer planes were used for thermal loading characteristics. PCBs of two different thicknesses (0.062" and 0.093") were used and two surface finishes - Immersion Ag and Ni-Au - are used in this investigation. The PCB was split into 4 sections, with each section consisting of a different via design.

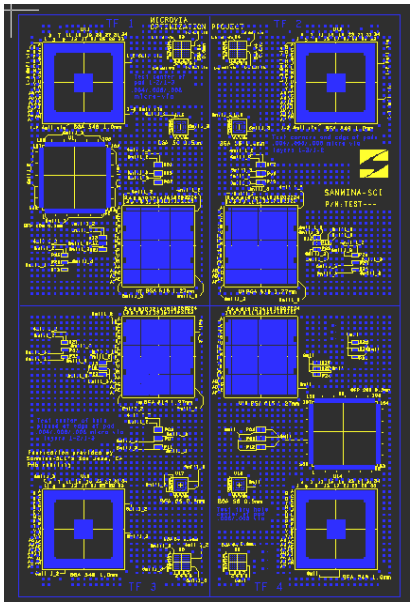
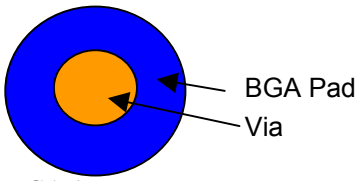


Figure 1: Via-In-Pad PCB

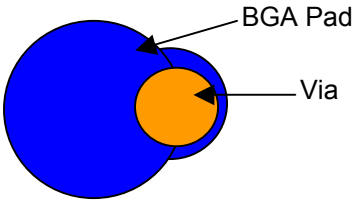
For this evaluation, the following components were used:

- 615 ball, 1.27 mm pitch BGA
- 548 ball, 1.00 mm pitch BGA
- 64 ball, 0.8 mm pitch BGA
- 56 ball, 0.5 mm pitch BGA
- 208 lead, QFP 0.5 mm pitch QFP
- 0805s, 0603s, and 0402s capacitors

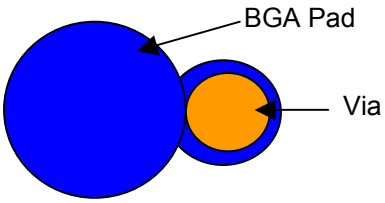
The different via designs for the BGAs are shown in Figure 2 below. BGA 1 was used twice in the design – once for a micro-via and then again for a through hole configuration. See Table 1 for a complete list of the designs used. The images below show the BGA pad styles used and via-holes.



BGA 1



BGA 2



BGA3

Figure 2: BGA Design Patterns Used

The via-hole design for the QFP is shown in Figure 3. For the QFP only 1 via-hole location was used.

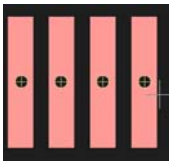


Figure 3: QFP Design Patterns Used

The via-hole design for the passive devices is shown in Figure 4:

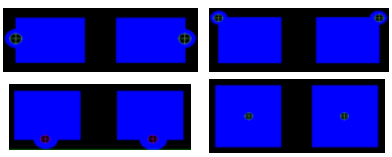


Figure 4: Passive Design Patterns Used

Via-Hole sizes being tested include 4, 6, and 8 mils and these go from layer 1 to layer 2 and from layer 1 to layer 3 of the PCB. A through-hole configuration is also included for each device i.e. these vias went for layer 1 to layer 8 of the 8 layer PCB.

Device	Pitch in mm	Lyr 1 to 2 (mils)	Lyr 1 to 3 (mils)	PTH (mils)
BGA 548	1.0	4, 6	6, 8	8
BGA 615	1.27	4, 6	6, 8	8
BGA 64	0.8	4, 6	6, 8	8
BGA 56	0.5	6	6	8
QFP 208	0.5	4, 6	6, 8	8
Passives	n/a	4, 6	6, 8	8

Table 1 – Overall Design Parameters

The boards were assembled on a standard production SMT line and the primary goal of this build was to look at the influence that the via-hole location and size had on solderability, if any. The main measurement criteria would be to look at solder joint voiding issues that are typically associated with the use of this type of design.

A standard no clean solder paste (63/37 SnPb) was chosen for the purposes of the investigation. A stencil design that had been used successfully in the past was incorporated and used along with a reflow profile that has been known to minimize solder joint voiding. This was done since there would be no variation of any of the assembly parameters during the run. The goal was to look at optimizing the design criteria when using a via-in-pad layout.

Some of the production parameters:

- One stencil design was used for all boards. The stencil was 5 mils thick and the apertures were designed to be 1:1 with the SMT pads.
- Average paste height recorded was 5.8 mils, which is acceptable.
- Oven set points varied from the .062 board to the .093 board but a single profile, as measured by solder joint temperatures, was used.
- Based on the chosen solder paste a straight line preheat / soak cycle and then a spike to 215 degrees was used as our reflow profile. (See Figure 5)
- All reflow was done in an air environment

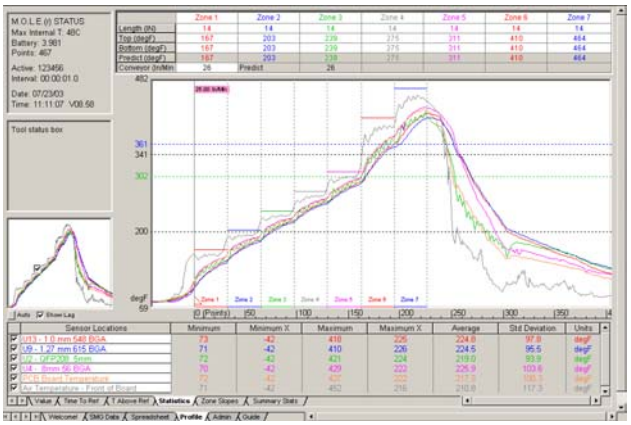


Figure 5: Reflow Profile

The assembled boards covered 2 surface finishes and 2 board thickness. As stated earlier the evaluation criteria will be the examination of solder joint voiding, and as such X-Ray analysis will be used to observe the results.

TESTING & RESULTS

Our primary analysis tool was the use of X-Ray inspection, both transmission and Laminography, to look at void size and location in the solder joint. Although the board contained passives and QFP's, the analysis concentrated on the BGA's used on the assembly. There is no specific IPC pass / fail criteria for BGA voiding. The paragraph below is taken from IPC-610C and serves as a guideline or reference point:

The following guidelines are provided as assessment criteria for the attachment technology process. Without substantial documented reliability data at the time of publication of this revision, no acceptability criteria are provided.

Acceptable - Class 1, 2, 3
• Less than 10% voiding in the ball to board interface.

Process Indicator - Class 2, 3
• 10-25% voiding in the ball to board interface.

Voiding in the BGA solder ball to board interconnection up to 25% may or may not be a reliability issue and should be determined in your process development. BGA solder joint reliability studies performed at some industry locations show that limited voiding in BGA balls does not impact long-term reliability.

Defect - Class 1, 2, 3
• More than 25% voiding in the ball to board interface.

With this specification open to some interpretation the point of this analysis will be to compare the various design configurations to each other and whether or not it is a reliability issue will not be looked at.

Transmission X-Ray Images:

Figure 6A shows a 0.5 mm BGA. All pads were designed with 6 mil vias in the center of the pads. On the left side the vias go from layer 1 to layer 2 and on the right side the vias go from layer 1 to layer 3. Notice the increase in voiding as the depth of the via hole increases. Figure 6B shows the same package but the sample, in this case, has an 8 mil through hole via. (Layer 1 to the bottom of the PCB).

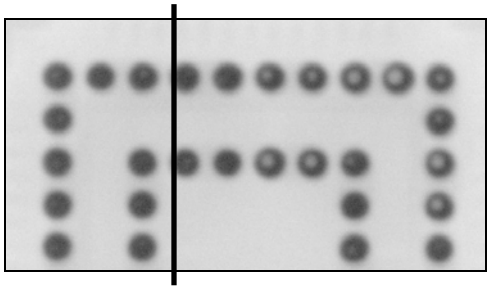


Figure 6A: 0.5 mm BGA

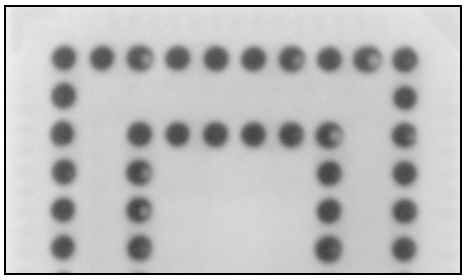


Figure 6B: 0.5 mm BGA

Figure 7 shows a 0.8 mm BGA. All pads were designed with 8 mil plated through holes going from layer 1 to the bottom of the PCB (layer 8) in the center of the pad. Notice the large voids throughout the entire device very similar to the 0.5 mm pitch package.

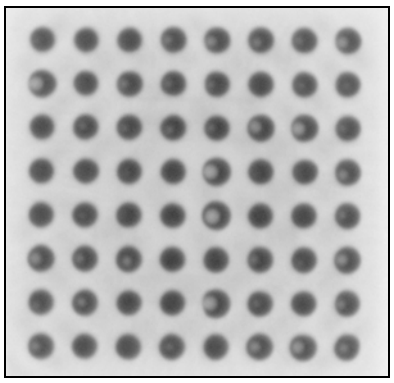


Figure 7: 0.8 mm BGA

Figures 8A and 8B are images of a 1.0 mm BGA. Both use a 4 mil via–in-pad going from layer 1 to layer 2. The top image (Figure 8A) has the via-hole in the center of the pad while the second image (Figure 8B) uses a via-hole offset from the center of the pad. Voiding was reduced by using the offset via-hole configuration.

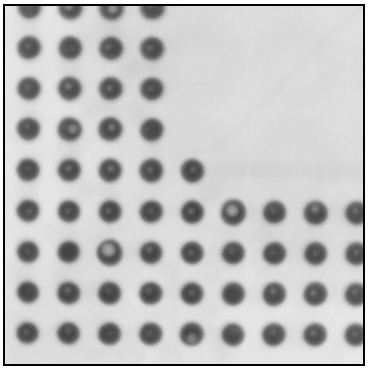


Figure 8A: 1.0 mm BGA

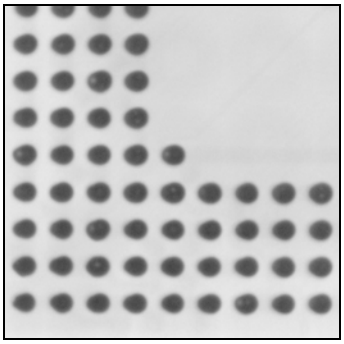


Figure 8B: 1.0 mm BGA

Laminography X-Ray Testing:

Three locations were examined in the BGA solder joints using Laminography – See Figure 9:

Slice # 1: Center of the ball
Slice #2: Interface between ball and BGA substrate
Slice #3: Interface between the ball and the PCB

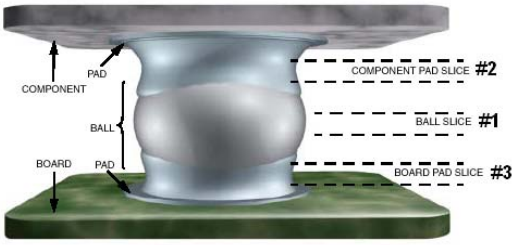


Figure 9: Laminography Slices (image courtesy of Agilent)

Each measurement tested for: the presence of voids, the number of voids, the size of the voids, and the location of the voids. Figure 10 shows an example of BGA void cross section.

The data generated from the Laminography testing was fairly extensive and was parsed based on the following criteria:

- Board Surface Finish
- Board Thickness
- Board Pad Design
- Component Type
- Via-Hole Size
- Layer 1 to Layer 2 Via-Hole
- Layer 1 to Layer 3 Via-Hole

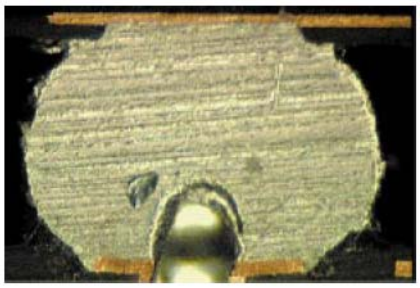


Figure 10: Example of BGA Void

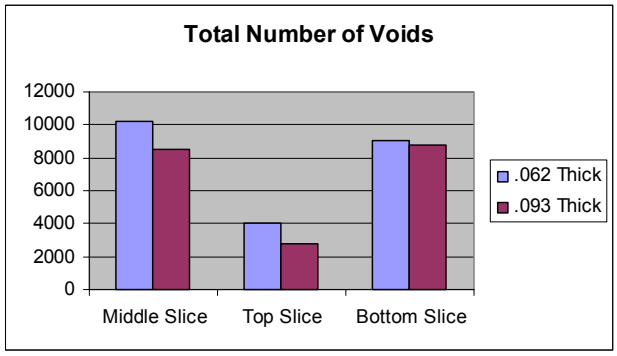
This was performed for each of the measurement slices looking to determine the effect of each variable. Measurements were taken and recorded on the Laminography equipment and then calculations were performed for the mean void size, the standard deviation, the range, the minimum void size, the maximum void size, and the number of voids.

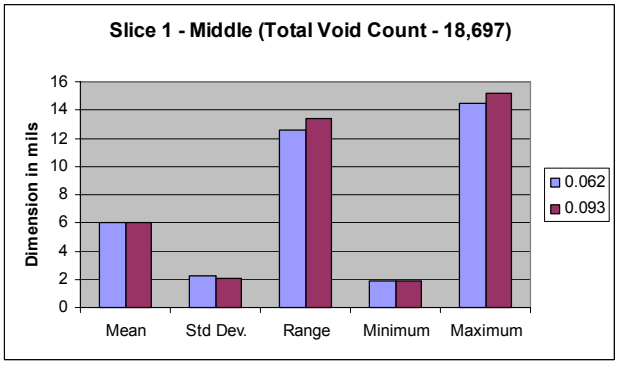
Definitions for the charts with all units being in mils:

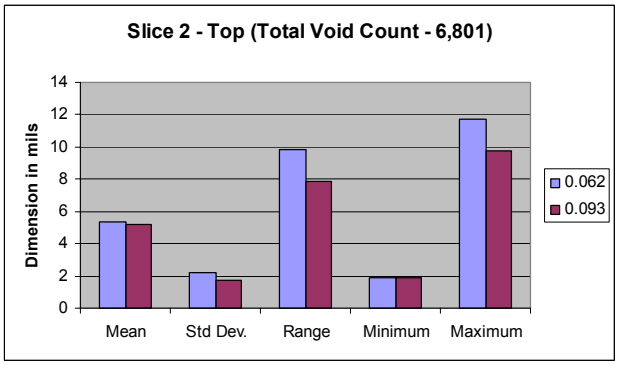
- Mean – Standard mean calculation for the via-hole size
- Std. Dev. – Standard Deviation for the via-hole size
- Range – Largest via-hole minus the smallest
- Minimum – Smallest void size
- Maximum – Largest void size

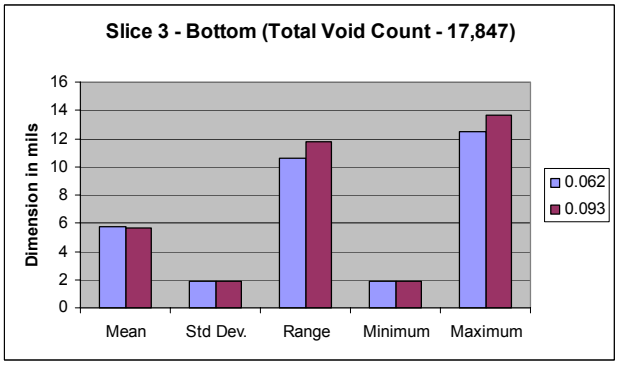
Test 1: Effect of Board Thickness

In general the .093 boards produced less voiding than the .062 boards. The mean and standard deviation for the voids were close in each thickness but the total voids found numbered about 15% higher for the thinner boards. All other data showed little variation. Further work will be done in the next phase of this project to analyze the cause of this difference.



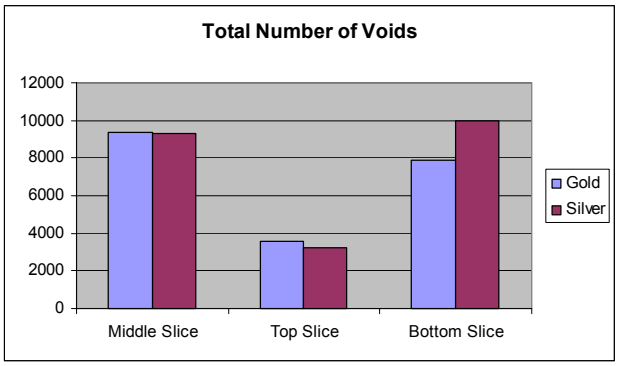


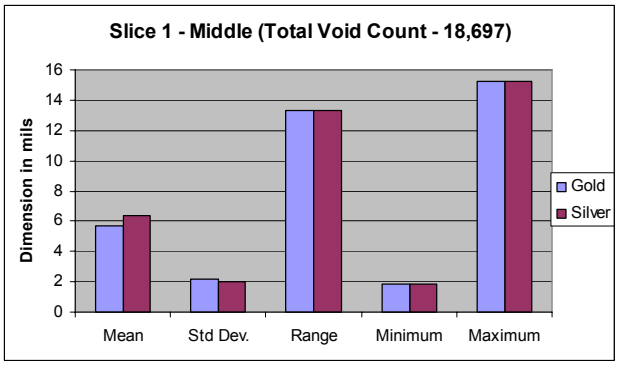


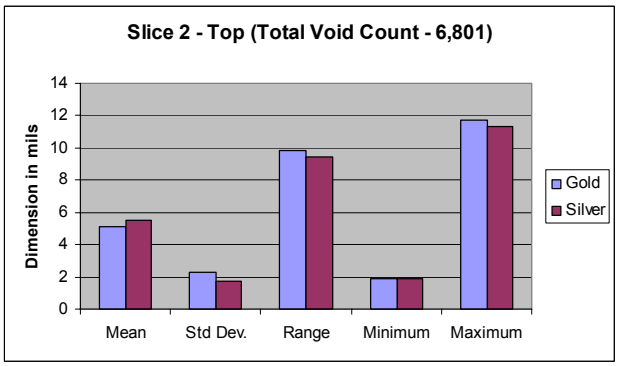


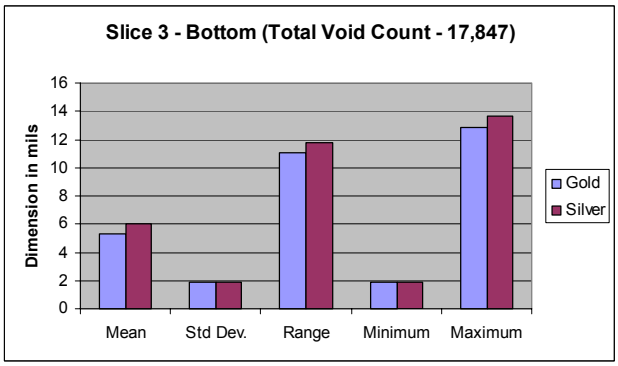
Test 2: Effect of Surface Finish

There was varying data for the surface finish comparisons. Mean and standard deviations were fairly close but there was about a 25% increase in the number of voids for the bottom slice on the boards with Immersion Ag plating.





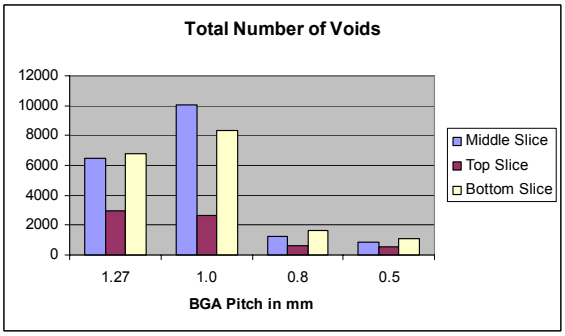


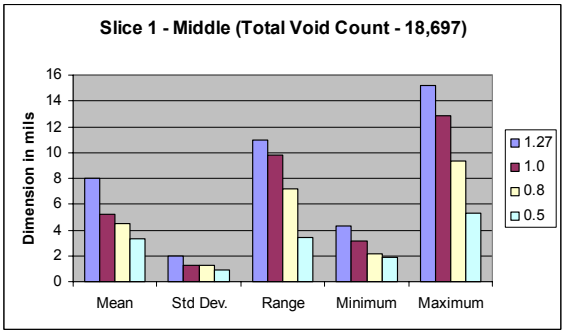


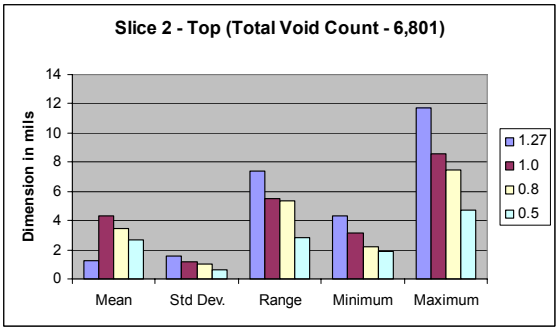
Test 3: Effect of Component Type

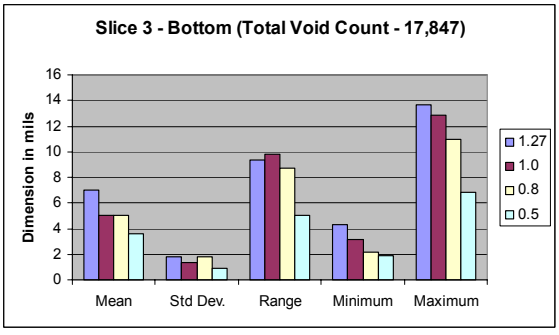
For the component type data a normalization of the data was performed. There are 4 of each BGA type on the PCB but the I/O count drops as the pitch decreases. To compensate for the decrease in the number of solder joints it was assumed that the data distribution was fairly normal and did a straight multiplication for the number of voids.

The results when using this normalization shows that there is an increase in the number of voids although they do decrease in size. This is to be expected since the via-hole sizes are held constant and become a larger percentage of the pad volume as the pitch decreases.





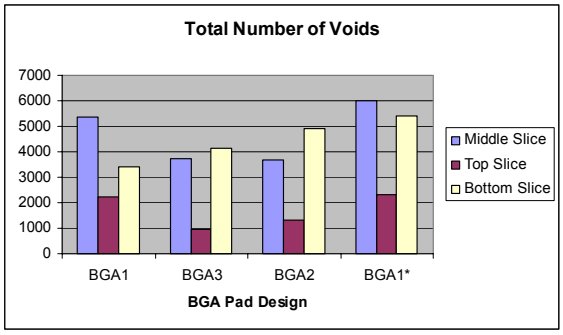


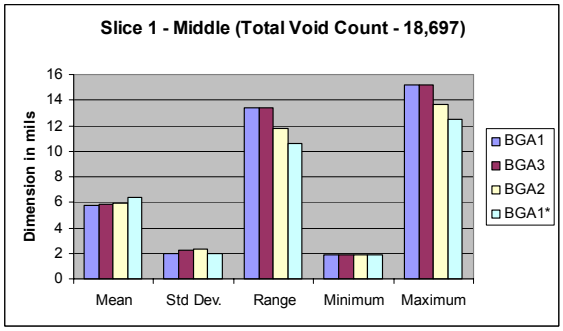


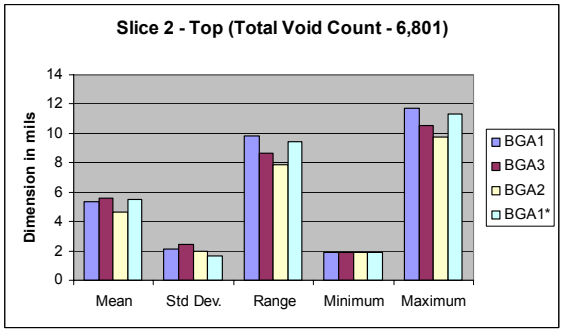
Test 4: Effect of Pad Design

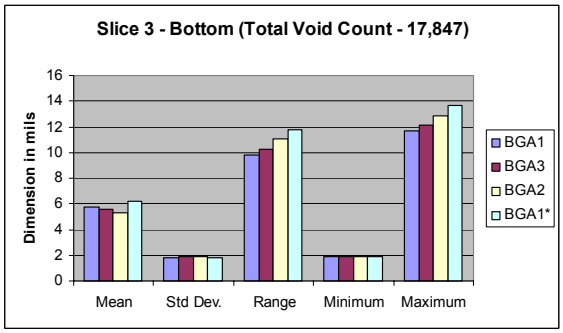
See Figure 2 for a description of the pad designs. BGA1* is the BGA1 Pad Design with the via-hole going through the board – top to bottom.

Void formation for the pad design changes varied by location of the void in the ball. BGA pattern 1 produced the most voids when looking at the middle slice but the least when looking at the bottom slice. BGA pattern 2 produced the highest when looking at the bottom slice. Overall BGA pattern 3 produced the least amount of total voids. The highest voiding was present using pattern BGA1*. The mean and standard deviations were fairly close across the pad designs.



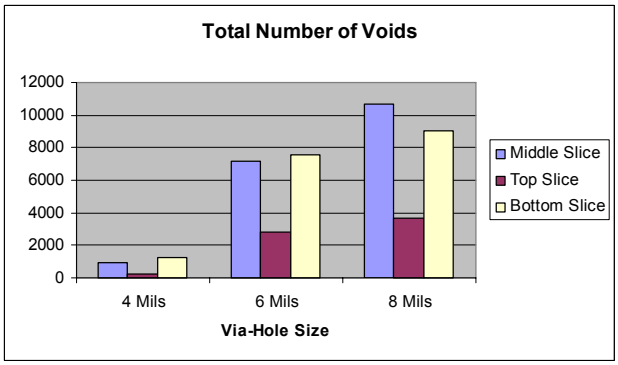


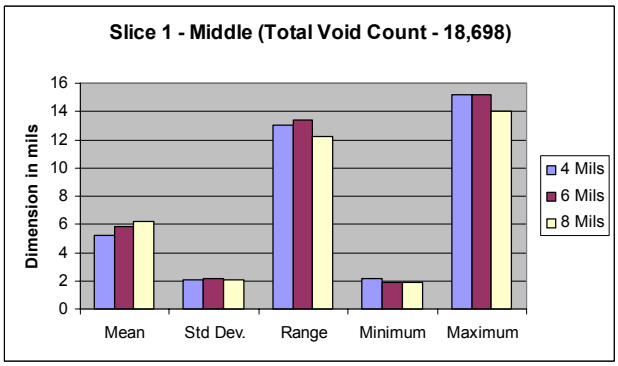


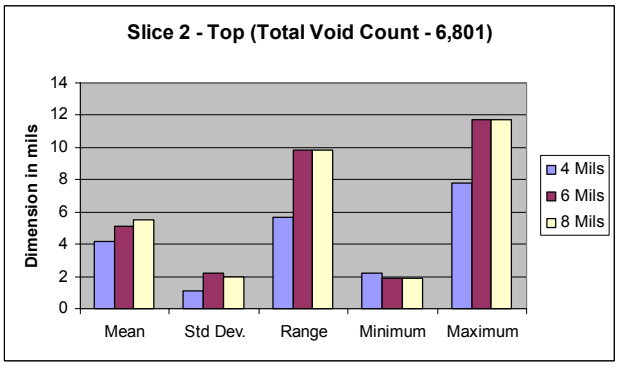


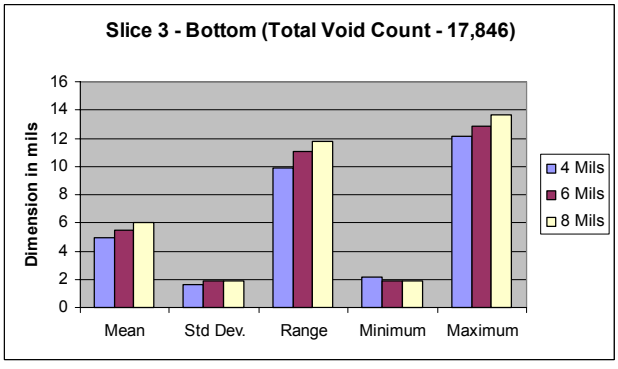
Test 5: Effect of Via-Hole Size

The via-hole size showed one of the largest effects of this experiment. Using a 4 mil via-hole produced much lower void counts at all layers of the BGA ball.



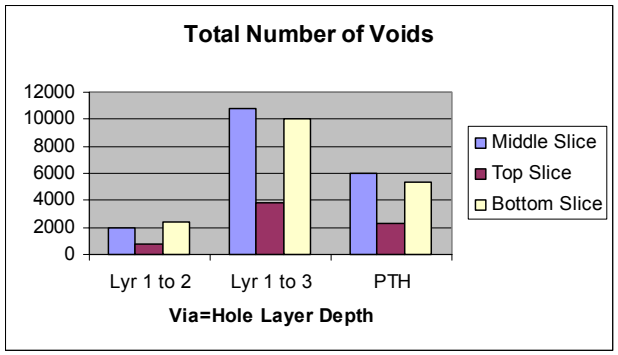


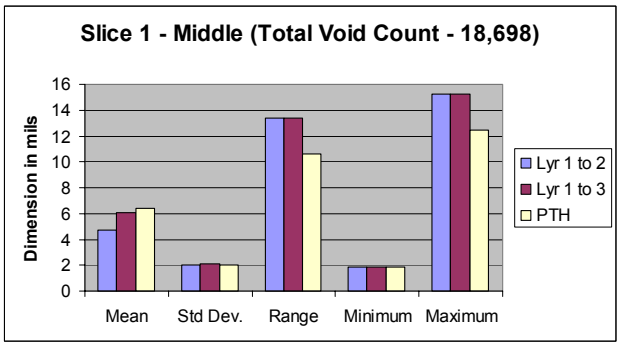


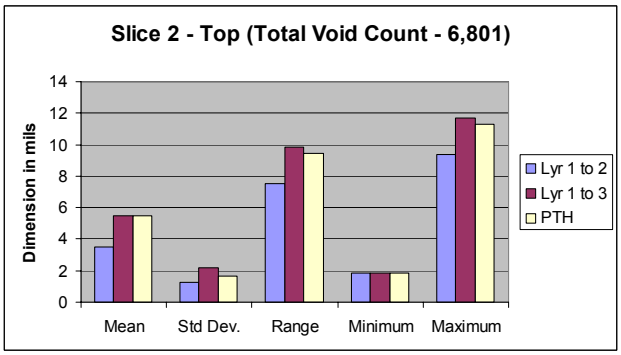


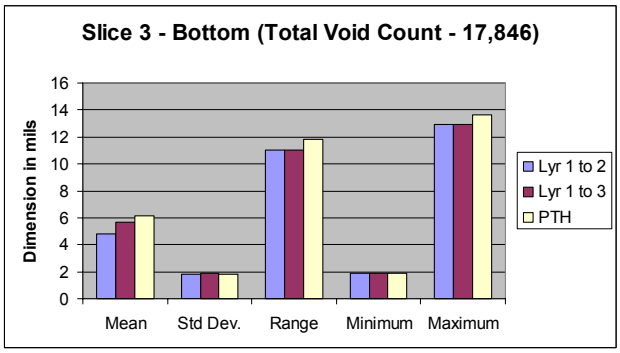
Test 6: Effect of Via-Hole Layer Depth

Via layer depth is defined as the starting and ending layer of the via-hole. PTH defines a via-hole going through the entire board – in this case layer 1 to layer 8. Via-Hole layer depth showed much lower voiding for going from layer 1 to layer 2 than for layer 1 to layer 3. The PTH via-holes did show lower voiding than layer 1 to layer 3.









SUMMARY OF RESULTS

- In general the .093 boards produced less voiding than the .062 boards. Approx. 15% difference was observed.
- There were about a 25% increase in the number of voids for the bottom slice on the Ag versus Au boards.
- With the exception of the 1.27 mm BGA as pitch decreased so did the occurrence of voids. There was a large decrease as the pitch went down to .8 mm and then a slight decrease as the pitch went from .8 mm to .5 mm.
- The location of the via-hole had an effect on void formation. With the via-hole located in the center of the pad (for both through hole and micro-via) there was an increase in voiding. As the via-hole moved further away from the center of the pad, voiding decreased.
- The via-hole size had a dramatic effect on void formation. Out of all voids found, the 4 mil via accounted for 6% of the total. This was followed by the 6 mil via-holes, which accounted for 40% and then the 8 mil via-hole at 54%.
- Via-Hole layer depth also proved to have a large impact on void formation. Out of al the voids found the layer 1 to layer 2 via-holes accounted for 12% of the total. Next in number was the through hole via at 32%. The largest percentage came from the via-hole going from layer 1 to layer 3 with 56% of the total.

CONCLUSIONS

The optimum VIP design is one where the via-hole location is offset from the center of the pad and as small as possible.

Based on current IPC 610-C guidelines for solder joint voiding, using BGA patterns 2 & 3 (see Figure 2) will meet the 25% criteria stated. For the other pad designs mixed results were observed and further analysis needs to be performed on these pad designs.

The conclusions given here are based on assembly criteria only and another phase of this project will address the PCB issues. In addition to further analyzing the results obtained so far additional work will be required to address the impact on high volume manufacturing.

REFERENCES

[1] Arledge, K. and Swirbel, T., "Microvias in Printed Circuit Boards", www.ipc.org/html/s08-1.pdf, 1998, pp. S08-1-1 - S08-1-9

[2] Burgess, L. and Madden, P., "Putting Blind Vias in SMD Pads: Where They Belong", Proceedings - Surface Mount International, www.laservia.com/PDF/smi97.pdf, September 1997

[3] IPC, "Design Guide for High Density Interconnects (HDI) and Microvias", IPC/JPCA-2315, Illinois, June 2000.

[4] Gonzalez, C., "High Density Interconnection", CircuiTree Magazine: The Board Authority, Volume 1, Number 2, June 1999.

ACKNOWLEDGEMENTS

The authors wish to thank the other individuals involved in this project: Lynn Shaver and his Engineering staff for assisting with the assembly of the boards and James Loverich for his help with the x-ray laminography testing.