# BOARD LEVEL RELIABILITY OF LEAD-FREE PACKAGES

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**ABSTRACT**
Due to recent legislation and market trends, it has become imperative for component suppliers to provide lead free packages. Most lead free replacement alloys place higher demands on package material sets due to the required higher reflow temperatures. This condition results in different material sets, assembly processes, and pre-conditioning requirements for packages. Of course, providing a package that can meet these stringent reflow and pre-conditioning requirements while still maintaining acceptable package level reliability is not enough, as the impact to board level reliability is also a primary concern. The actual impact of these different lead free replacement alloy systems on the board level reliability is not well understood, especially across the different package types.

This study focused on the board level reliability of lead free replacements for all significant package families: Ball Grid Array's (BGAs), Chip Scale Packages (CSPs) and leaded packages. In order to execute this study, a partnership was formed between industry leaders in package assembly, board fabrication/assembly, solder alloy supplier and an OEM. Through this partnership, the mounting of the lead free components was analyzed and the board level reliability assessment was begun to match end user requirements.

Thus, this study aims to provide a comprehensive picture of board level reliability and a solution that the end users can implement to meet their immediate needs. The results obtained so far suggest that a reliable and robust solution is available for certain segments of the industry.

Key words: Lead-free, board level reliability, thermal cycling, solder joints.

**INTRODUCTION**
The lead-free initiative impacts all the segments of the manufacturing supply-chain. The component supplier, board assembler, solder paste/alloy manufacturer and the original equipment manufacturer (OEM) must work together in-order to arrive at a workable solution that has a reliability equal to the current Sn/Pb system, if not higher. This paper assesses the reliability of the solder joints of various alloys/combinations subjected to accelerated temperature cycling (ATC) regimes in order to achieve an understanding of the solder fatigue mechanism. Additional benefits of such a test are an ability to predict solder joint life by modeling and simulation based on the accelerated transform obtained from the results and to understand the use environment [1].

Prior to the commencement of this study, the component level reliability at the higher reflow temperature was evaluated with the arrived upon material sets compatible with these temperatures [2]. A test vehicle was designed having six component types including BGAs and pre-plated Quad Flat Pack (QFP) leadframes (Nickel/Palladium/Gold). An experiment was designed to evaluate a number of scenarios. A board with multiple components having different solder ball alloys and a common solder paste on the board was selected. Different board materials were also included (high-Tg FR-4 and a polyclad material). The coefficients of thermal expansion (CTE) in the x, y and z direction were measured below the glass transition (Tg) temperature. The test boards were then thermal cycled in two temperature ranges, -40 to 125°C and 0 to 100°C to accommodate the different requirements existing in the industry.

Though testing is not complete the interim results indicate that zero failures are observed until 880 cycles in the 0 to 100°C range and 475 cycles in the –40 to 125°C range. For some segments of the industry these are acceptable numbers for beginning mass production.

**METHODOLOGY & MATERIALS**
The primary objective of the experiments was to gather a sufficient database on a wide array of package types. The multiple objectives of the study are listed below:

1. To determine the viability of assembling surface mount components on printed circuit boards using lead-free solder alloys.
2. To determine the solder joint reliability of the test assemblies.
3. To evaluate the reliability of multiple solder ball alloy compositions assembled with a common solder paste alloy.
4. To provide a production worthy process that meets the system level requirements.

Based on the above requirements the test vehicle was designed with a variety of package types, Table 1. All the packages had a daisy chained die in them. All the packages evaluated in this study have proven package level reliability at the 260°C temperature reflow [2].

| Package | Size (mm) | I/O | Pitch (mm) | Die Size (mils) |
|---|---|---|---|---|
| PBGA | 35x35 | 388 | 1.27 | 330x330 |
| PBGA | 15x15 | 196 | 1.0 | 330x330 |
| µBGA™ [1] | 6.3x6.2 | 48 | 0.75 | 236x338 |
| M2CSP™ [2] | 8x10 | 72 | 0.8 | 236x228 |
| EconoCSP™ [2] | 15x15 | 208 | 0.8 | 330x330 |
| MQFP (PPF) | 28x28 | 208 | 0.5 | 240x240 |

**Table 1.** Components on the test vehicle.

The type of tests to be conducted dictated the layout of the board. The 388 I/O PBGA was chosen as the component used for comparing the various solder ball alloys assembled with the Sn/Ag/Cu paste. The various solder ball alloys used in this study are listed in Table 2 (with recommended reflow temperatures). In addition, the four-point bend testing requires a particular arrangement of the test samples. This was also taken into consideration. The lead-free solder chosen for comparison to the eutectic Sn/Pb control was Sn/3.9Ag/0.6Cu. Process optimization runs were undertaken prior to the assembly. The assembly of the test vehicle was to be coordinated per the requirements of a new process qualification viz. average solder paste dispense volume measurements, 100% x-ray of solder joints, electrical testing of the assembled boards and acoustic microscopy to check for delamination in components.

| Leg | Composition | Melting Point (°C) | Max. Reflow Temp (°C) |
|---|---|---|---|
| 1 | Sn/37Pb | 183 | 210-220 |
| 2 | Sn/3.5Ag | 221 | 245-255 |
| 3 | Sn/0.75Cu | 227 | 250-260 |
| 4 | Sn/4.0Ag/0.5Cu | 217-218 | 240-250 |
| 5 | Sn/2.5Ag/1.0Bi/0.5Cu | 216-221 | 240-250 |

**Table 2.** Different solder ball alloys tested.

**Board Design and Material**

Given the need to have a test vehicle consistent with the requirements imposed by the various tests, a double-sided board was designed (Figure 1).

[1] µBGA™ is a registered trademark of Tessera, Inc.

[2] M2CSP™ & EconoCSP™ are registered trademarks of ChipPAC, Inc.

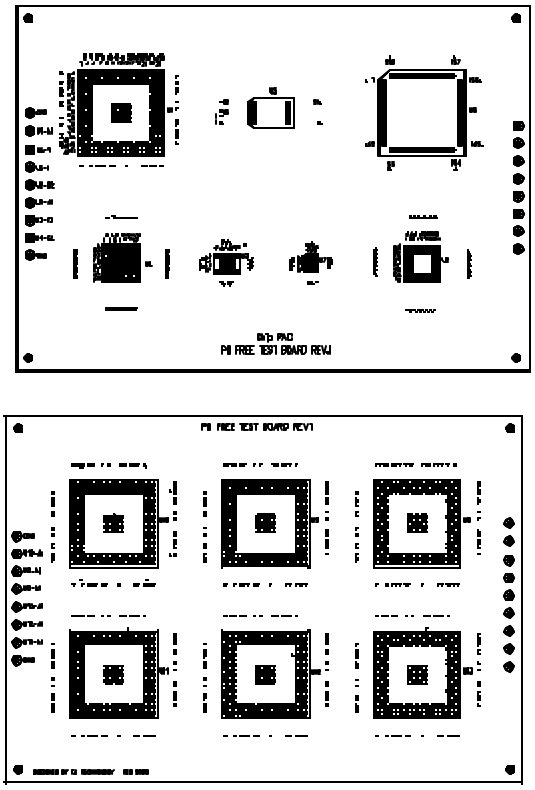

**Figure 1.** Topside and bottom-side layout of test vehicle.

The topside of the board was used to test six various packages types. The bottom side had six locations of the 388 I/O PBGA and was used for the comparison of the different solder ball alloys and for the bend testing experiment. This paper, however, deals only with the thermal cycling tests. The board design details are provided in Table 3.

| | |
|---|---|
| PCB thickness | 62 mils |
| PCB layers | 4 |
| PCB pad design | NSMD |
| PCB pad finish | Organic solder protect |

**Table 3.** Features of board design.

Each of the components had one daisy chain net associated to it with the intent of employing an in-situ monitoring. So, the entire package is considered to fail when the first solder joint fails electrically (defined by a resistance rise of 150-225 ohms depending upon the component tested). For the array packages, test points were also provided along the outermost row of each package so as to facilitate failure analysis by determining the solder joints that actually failed. This was done on the basis of prior knowledge of the probability of the failures occurring in the corner balls in the periphery of the package was the highest especially for peripheral array packages.

The boards to be used in the lead-free product will have to withstand the high reflow temperatures, thereby imposing a higher stress on the board layers. For this reason the standard FR-4 board was not used for the experiments.

Instead, the polyclad material was used as a base and a few boards using the High-Tg FR-4 material were also fabricated. The CTE in the x, y and z direction for the board material in the presence of solder mask was determined since the differential thermal expansion between the board and the components largely drives thermal fatigue of the solder joints. The standard FR-4 material was used as a reference base. The CTE's in the three directions were measured using thermo mechanical analysis (TMA) below Tg. The test specimens were preheated at 105C for two hours, cooled and stored. They were then tested on a Perkin-Elmer TMA7e from 25C to 200C using a 5C per minute heating rate in dry helium. The test results are tabulated in Table 4. Note that the readings are an average of two corners on the specimen. These results will help in modeling and simulations of the lead-free solder joint fatigue system.

| Sample | Axis | Tg (°C) | CTE Below Tg (ppm) |
|---|---|---|---|
| Std. FR-4 | X | 125.35 | 13.15 |
| Std. FR-4 | Y | 138.37 | 15.77 |
| Std. FR-4 | Z | 132.79 | 65.80 |
| High Tg FR-4 | X | 148.37 | 13.53 |
| High Tg FR-4 | Y | 144.93 | 16.97 |
| High Tg FR-4 | Z | 144.74 | 66.28 |
| Polyclad | X | 147.08 | 14.37 |
| Polyclad | Y | 142.77 | 17.37 |
| Polyclad | Z | 147.11 | 62.87 |

**Table 4.** Properties of board materials used in experiments.

**Board Assembly and Test**

Prior to the assembly of the test vehicles a comprehensive solder paste characterization study was undertaken. This included the printability study of a number of solder pastes with the no-clean and water-soluble flux. The results of these experiments will be published in an independent publication. Table 5 lists the materials used and the results of assembly. Note that acoustic microscopy suggests that no package delamination occurred during assembly (Figure 2)

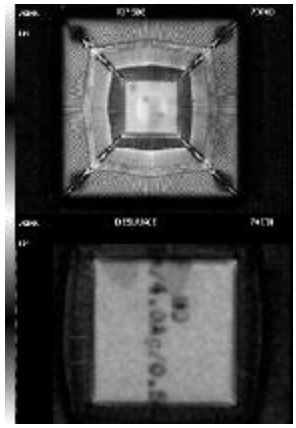

**Figure 2.** Acoustic microscope images of MQFP and EconoCSP™ package after board assembly at 249°C peak.

| | |
|---|---|
| Component pre-bake | 24hrs@125°C |
| Stencil thickness | 5 mils |
| Solder Paste | 63/37 Sn/Pb |
| | Sn/3.9Ag/0.6Cu |
| Flux | Water Soluble |
| X-ray inspection | 100% |
| Electrical test | 100% |
| Number of opens | 0 |
| Omega Meter readings | 3.7ug Nacl/sq.inches (Sn/Pb) |
| | 1.5ug Nacl/sq.inches (SAC) |
| Acoustic Microscopy to check for delamination in packages | No Delamination |

**Table 5.** Board assembly results.

Paste volume measurements were taken and a summary of the data is provided in Table 6.

| Package | Target Paste vol. (cubic mils) | Aperture Size (mils) | Actual Paste Vol. (Average) | |
|---|---|---|---|---|
| | | | Sn/Pb | Sn/Ag/ Cu |
| PBGA 388 | 2453 | 25 | 2375 | 2577 |
| PBGA 196 | 1271 | 18 | 1074 | 1114 |
| µBGA™ | 663 | 13 | 424 | 510 |
| M2CSP™ | 663 | 13 | 505 | 514 |
| EconoCSP™ | 663 | 13 | 489 | 543 |
| MQFP (PPF) | 3300 | 60x11 (rectangle) | 2913 | 3080 |

**Table 6.** Paste volume measurements.

The reflow profiles used for the assembly are shown in Figure 3.

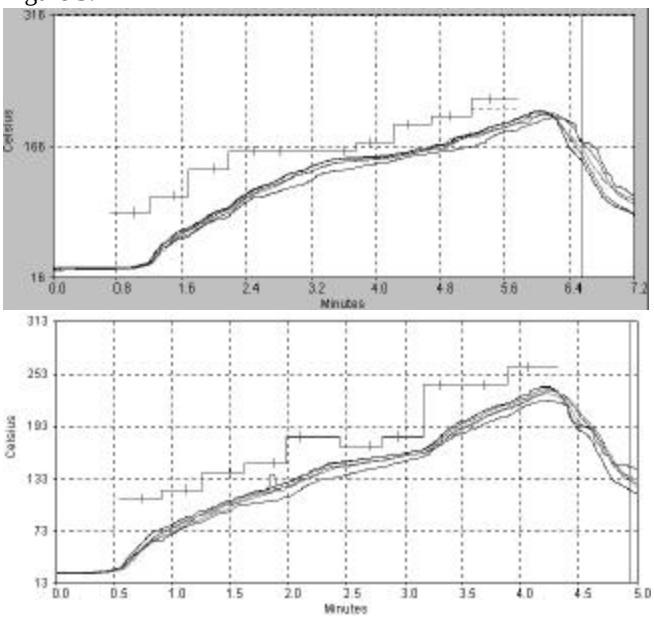


**Figure 3.** Reflow profiles used: Top - 63/37 Sn/Pb paste (220°C peak), Bottom - Sn/3.9Ag/0.6Cu (249°C peak).

The reflow profiles were arrived at after optimizing for the given components and the various ball alloys/surface finish on the board. The integrity of the components after the board assembly was not a concern because of the prior validation of the components at the higher temperature reflows. In-order to have the component data prior to the thermal cycling tests and also as a confirmation of the component level study [2] it was decided to have acoustic microscope images of a sample of components that have undergone the high temperature reflow. In addition, solder joint cross-sections were done at time-zero. Photomicrographs shown in Figure 4 illustrate the solder joints of a BGA and a MQFP.

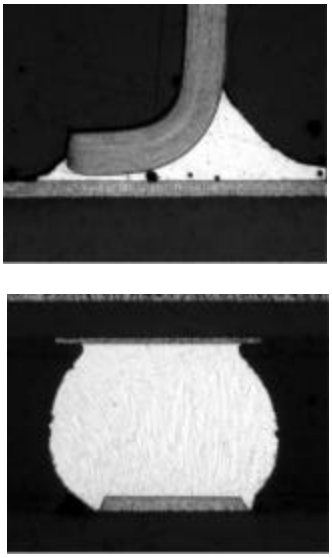

**Figure 4.** Top: Cross-Section of MQFP (Ni/Pd/Au – Sn/3.9Ag/0.6 Cu paste). Bottom: Cross-Section of BGA (Sn/3.5Ag sphere - Sn/3.9Ag/0.6 Cu paste).

The cross-sections indicate acceptable solder joints from the assembly process.

**LIFETIME PREDICTIONS**

The predictions made for the lifetime of a range of products help in comparing the results obtained from thermal cycling and thereby assist in deriving an idea as to the level of reliability attained by the components tested. The following calculations shown in Table 7 are based on the modified Norris-Landzberg equation [3]. The acceleration factor (AF) serves as a measure of correlation between the actual and the predicted cycles to failure.

$$AF = N_{field}/N_{lab} = (\Delta T_{field}/\Delta T_{lab})^{-1.9} \times (f_{field}/f_{lab})^{1/3} \times \{\exp(1414/T_{field\text{-}max} - 1414/T_{lab\text{-}max})\}$$

**Where:**

$AF$ : Acceleration Factor
$N_{field}$ : Number of cycles in the field
$N_{lab}$ : Number of cycles in test
$f_{field}$ : Frequency of on/off cycles for the product (minimum 4 cycles per day).
$\Delta T_{field}$ : $T_{on}$-$T_{off}$ (Assumed 30°C)
$\Delta T_{lab}$ : 100 (0 to100°C) & 165 (-40 to 125°C)
$f_{lab}$ : Frequency of cycles during test.
$T_{field\text{-}max}$ : Tjunction temperature of the device
$T_{lab\text{-}max}$ : 100 (0 to100°C) & 165 (-40 to 125°C)

It must however be noted that these comparisons serve only as an indication based on a certain set of assumptions. The actual in-life use conditions and parameters may vary.

**THERMAL CYCLING TESTS**

Electronic packages of the type considered in this study find applications in varied segments of the industry, some demanding high solder joint reliability and others for which low reliability is acceptable. Therefore, two temperature ranges were selected for accelerated thermal cycle testing. Thermotron® temperature chambers equipped with Hewlett Packard E1346A data acquisition systems were used for the experiments. The various components tested had different resistances therefore the expected resistance rise associated with a failed solder joint ranged from 150 ohms to 225 ohms.

Additional number of unconnected boards (assembled with daisy chained components) was also placed in the chambers for the purpose of conducting dye penetrant tests on the sample type that fails at a particular cycle so as to determine the interface and cause at the particular instant. This technique enables continuing tests without any stoppage time associated with isolating the failed component from the test vehicle. The experimental matrix is shown in Table 8.

| Product | on/off cycles A | Accl. Factor | | Design life (years) B | Test cycles C=A*B | Safety Factor D | Cycles E=C*D | Equivalent cycles | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0to100°C | -40to125°C | | | | | 0to100°C | (-40to125°C) |
| ES | 2/month | 4.3 | 22.3 | 15 | 360 | 2 | 720 | 168 | 32 |
| HES | 3.5/week | 4.3 | 22.3 | 12 | 2016 | 1.5 | 3024 | 704 | 136 |
| PC | 1/day | 4.3 | 22.3 | 7 | 2555 | 1.5 | 3832.5 | 893 | 172 |
| CE | 2/day | 4.3 | 22.3 | 5 | 3650 | 1.5 | 5475 | 1275 | 245 |

**Table 7.** Equivalent lifetime calculations (ES: enterprise server, HES: high end server, PC: personal computer, CE: consumer electronics). Note: The number of test cycles in this table is not an indication of any product qualification requirements.

| Paste | Component types | Side | Qty | Serial Numbers |
|---|---|---|---|---|
| Sn/Pb | Sn/Pb BGAs and Ni/Pd/Au leaded comp. | top | 64 | ATC –40~125: 1-32 ATC 0~100: 33-64 |
| Sn/Ag/Cu | Sn/Ag/Cu BGAs and Ni/Pd/Au leaded comp. | top | 64 | ATC –40~125: 65-96 ATC 0~100: 97-128 |
| Sn/Ag/Cu | Sn/Pb, SAC, SACBi, Sn/Cu, Sn/Ag BGAs | bottom | 64 | ATC –40~125: 129-160 ATC 0~100: 161-192 |

**Table 8.** Experimental test matrix for thermal cycling.

The parameters for the temperature cycling are given in Table 9. These parameters are as per the JESD22-A104-A temperature cycling standard and have been modified to have a tighter tolerance range by the lead-free consortium run by NEMI® for its board level reliability tests. A sample size of 32 boards was selected to provide accurate determination of the weibull slope and characteristic life.

| Condition | 0~100°C | -40~125°C |
|---|---|---|
| Min Temp | 0°C | -40°C |
| Max temp | 100°C | 125°C |
| Ramp | 10 °C/min | 11°C/min |
| Dwell at T-high | 10 mins | 15 mins |
| Dwell at T-low | 10 mins | 15 mins |
| Cycle Time | 40 minutes/cycle | 60 minutes/cycle |

**Table 9.** Thermal cycling test conditions.

**RESULTS**

Interim results of the continuing temperature cycling are shown in Table 10.

| Test Range | No. of Cycles | No. of Failures |
|---|---|---|
| 0 to 100°C | 880 | Zero |
| -40 to 125° C | 475 | Zero |

**Table 10.** Interim test results.

On comparison with the values calculated in Table 7 it can be seen that the current results suggest that the test assemblies have achieved levels of reliability demanded by certain segments of the industry.

**CONCLUSIONS**

Two sets of conclusions can be drawn; one from the assembly of the test assemblies and second from the thermal cycling.

Assembly:

1. The high temperature reflow did not cause delamination in the packages assembled.
2. X-ray inspection after assembly indicated no opens and shorts. Therefore, the lead-free solder paste on the OSP surface finish is acceptable.
3. Reflow of the lead-free alloys using a nitrogen-less convection oven is possible.
4. The assembled boards did not exhibit warpage issues.
5. All the components assembled had electrical continuity.
6. Existing equipment sets are capable of processing lead-free assemblies reliably.

Tests:

1. For the tested components, no failure was observed after 880 cycles between 0 to 100°C and after 475 cycles for the testing range between –40 to 125°C for both the control Sn/Pb paste and Sn/Ag/Cu paste.
2. The interim results suggest that there is no difference in the reliability among the various lead-free solder joints tested.

**FUTURE WORK**

The ATC tests will be completed and weibull plots will be generated for all the component types tested. Dye penetrant analysis will be performed on the test assemblies. Parallel aging and bend testing experiments are underway and on completion, comprehensive analysis work will be undertaken. The joint working group will also extend this program to Phase 2 wherein additional package types, no-clean paste and other parameters that were not considered in this current phase will be included.

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