

# SURFACE MOUNT TECHNOLOGY ADVANCEMENTS IN 2015

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People take for granted that electronics technology advances at a breathtaking pace—particularly in consumer electronics. But OEMs in telecommunications and mission-critical applications, such as medical and aerospace, are also demanding increased speed and new technology in the PCBs and PCBA's required for their latest products. Years ago, these advancements in technology would have been developed in many instances by major OEMs. But now, OEMs have come to depend on EMS providers to make the necessary advances in core technologies and processes in order to deliver these innovations.

SMT is evolving as a result of new components coming into the market. In the early 1980s, a 64-pin grid array (PGA) was considered a high pin-count device. In 2014, BGA (Ball Grid Array)

devices are in production with up to 3,700 terminations. Similarly, bottom terminated components (BTC) evolved in the 1990s from having just a dozen pins to 200-300 pins today.

Meanwhile, pad pitch continues to shrink, going from between 1 mm and 1.5 mm several years ago to production pitches of 0.4 mm or less today. Pad pitch limitations are driven by various factors, namely PCB via pitch, via technology (e.g., stacked vias) and line pitch currently between 2.5 and 3 mils for most production PCBs. Another driver is speed, increasing power and mixed signal integration with power and ground pins for different power domains. Also, PCB designers want passive components as close to a chip's power and ground pins as possible to improve decoupling. Finally, PCB technology is being driven to minimize chip-to-chip spacing in order to increase speed and signal

integrity. Increasing performance at a lower cost drives demand for BTC. These designs with tighter chip and component spacing however, present challenges if rework is required.

Tier 1 OEMs have increasingly turned to vertically integrated EMS providers to develop the technologies needed to bring complex, high performance products to market. Some of the key technology challenges OEMs and EMS providers are working to solve include: minimizing voids in BTCs; reducing the pitch between components while reserving sufficient space for rework; eliminating head-on-pillow defects in connections; and improving the robustness of PCBs used in high-temperature and/or corrosive industrial environments such as oil and gas exploration.

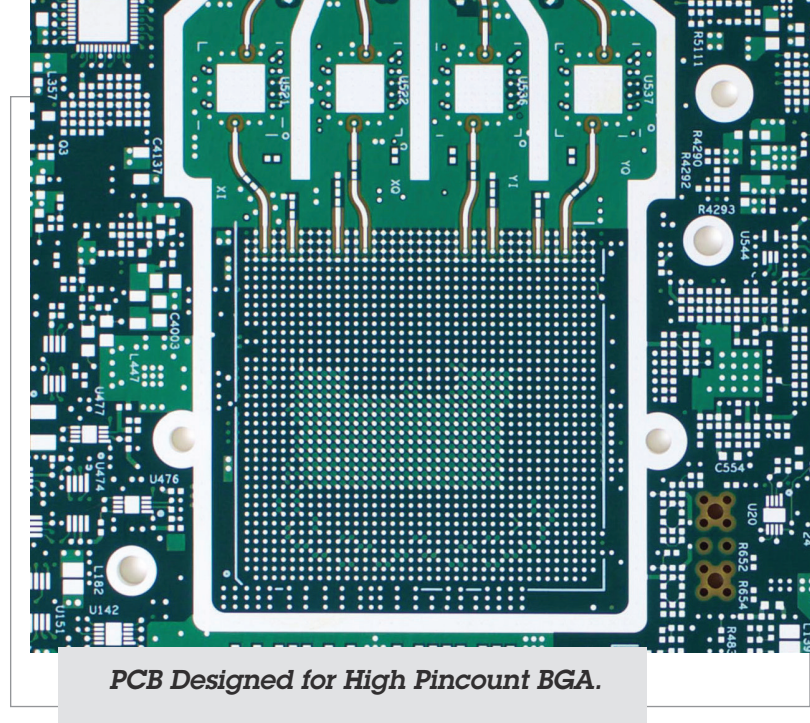
These issues continue to drive extraordinary advances in SMT processes as the number of terminations increase and pad pitch decreases. Here is a review of some SMT technology advances in 2014 and a look ahead to the challenges in 2015.

### **Challenge No. 1: Reducing Voiding in BTCs**

PCBs with BTCs are increasingly common, as BTCs have the advantage of offering good performance-both in signal integrity and thermal performance-at a relatively low cost. However, increasing pin count and package size and reduced pitch on BTCs creates production challenges. The increased pin count allows more functionality, and manufacturing faces new challenges in producing reliable contacts with these large-surface-area devices.

The biggest challenge with BTC packages is thermal pad voiding. During the solder reflow process, chemicals or air can be trapped in the solder, creating voids that may impact thermal conductivity or solder joint reliability. Large voids can result in early product failures or long term reliability risks. Thermal pads present a unique challenge during reflow, as the pads are typically larger and connected to large copper areas within the PCB, and therefore taking longer to reflow than solder balls associated with signal pads.

As we enter 2015, stencil design techniques, soldering materials, new processes and design for manufacturability practices are continuing efforts being practiced and fine-tuned to minimize voiding, while vacuum reflow is also being investigated with promising results.



### **Challenge No. 2: Rework Challenges Rise as Components Spacing Decreases**

OEMs are focused on functionality and performance. The use of decoupling capacitors for noise reduction leads to designs with more interconnects and smaller components with tighter component spacing. New designs, with more demanding signal integrity requirements can result in conflicts between layout requirements and what can be manufactured.

With the conflicts between design requirements and process capability, rework is becoming a challenge. For some high-performance computing and telecommunications PCBAs we produce at Sanmina, for example, the cost of a single PCBA may be over \$15,000. Therefore, it is imperative that the assembly is not damaged during rework. Furthermore, adequate spacing between components is also required to ensure that heat used for rework does not damage the solder joints of adjacent components, or the components themselves.

While IPC standards do not provide strict requirements for component spacing, and current SMT assembly processes can accommodate tight spacings, experience has shown that at least 200 mils of space should be left around large ball-grid arrays to allow for rework. OEMs are placing decoupling capacitors as close as 40 mils in order to optimize noise performance. EMS companies are working with equipment manufacturers to develop processes and rework tooling that make reliable,

repeatable rework possible, without inducing secondary reflow or additional rework of adjacent components. Although current solutions exist for keep-out space values well below 200 mils, additional process development and tooling enhancement are necessary to achieve tighter component spacing.

### Challenge No. 3: Chip Package Warpage

To minimize cost, ICs are often mounted in plastic packages. However, plastic is less stable for example than ceramic. When plastic packages are exposed to high temperatures during reflow, the package can warp: 2-10 mils or more, depending on the substrate, plastic material properties, package thickness and package size. A combination of package and PCB substrate dynamic warpage, along with PCB pad solderability issues, variations in printed solder paste volume can result in solder defects between a device and the PCB. Two common defects are head-on-pillow (HOP), or non-wet open (NWO) type defects.

While NWO defects create solder joints with no electrical continuity, HOP defects can be intermittent and/or unreliable. Therefore, testing for HOP defects is a challenge and as such, time-consuming and resource-intensive screening processes are needed in order to prevent products with these defects from getting into the field.

The JEDEC specification for package warpage, revised in 2005 and republished in 2009, allows for maximum of 8 mils of co-planarity at room temperature. Component suppliers usually provide specifications for room temperature co-planarity, using either the seating plane or regression plane measurement method. As long as the value is under 8 mils, the co-planarity is deemed within specification.

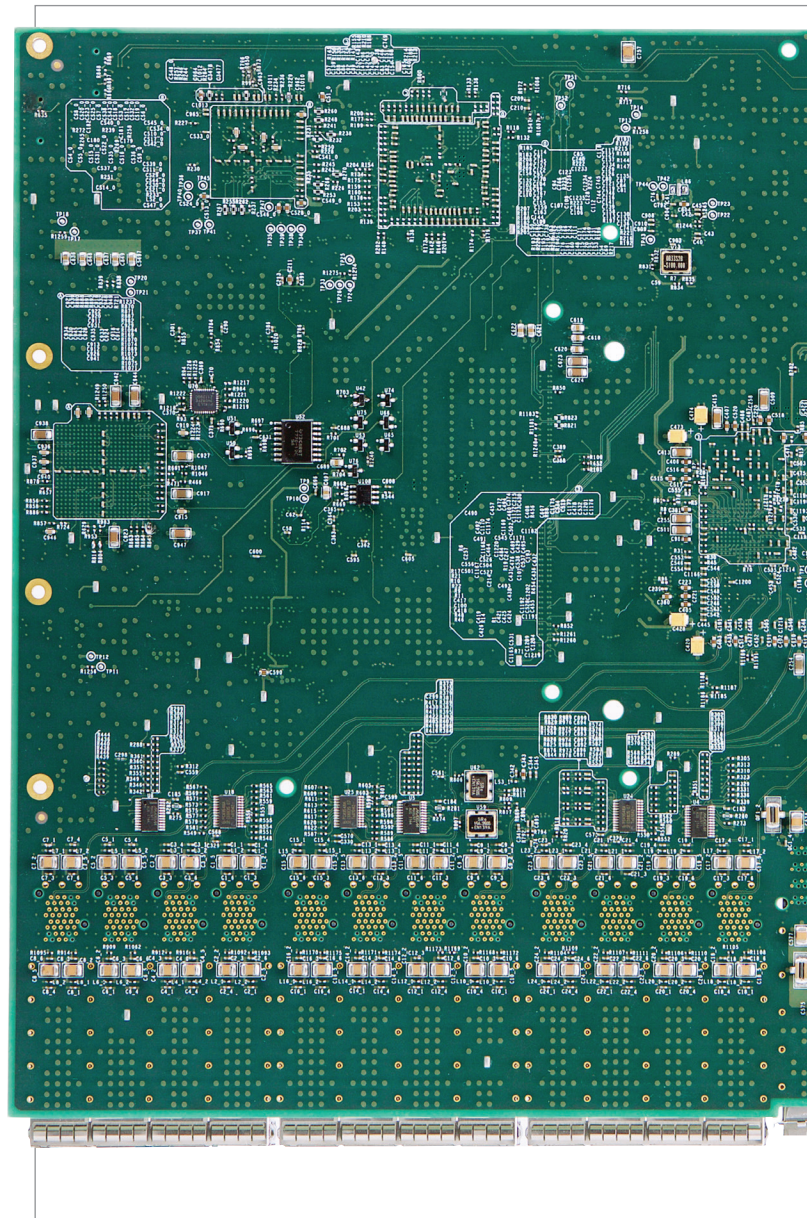
Empirical data suggests that the JEDEC specification is no longer adequate. For high pin count packages with small pads and lower solder volumes, production data suggests that component warpage exceeding 3.5 mils can cause problems during reflow, with a high potential for HOP defects. Manufacturers of consumer devices may discard or recycle defective boards, but this is not an option for an advanced computing or communications PCBA costing over \$110,000. Time consuming and expensive 3D X-Ray testing is necessary with assemblies susceptible to HOP defects.

In 2015, EMS providers will continue to drive

changes including advocating for improved plastic material compounds, along with working with JEDEC to tighten the standard warpage specification to closed to 3.5 mils for high pin count devices.

### Challenge No. 4: Building PCBAs Robust Enough for Mission-Critical Industrial Environments

Industries such as oil and gas use electronic assemblies in very demanding environments. Drilling and exploration tools used two to three miles below the earth's surface can cost upwards of \$2 million, and operate in environments up to 350F. This research will continue in 2015, as OEMs and EMS companies work to develop better materials and processes.



## Looking Ahead

SMT will continue to push the competing technical boundaries of signal integrity, miniaturization and increasing I/O counts. While devices with pad pitches in the range of 0.3 mils are already being assembled with automated surface mount equipment, this pad pitch cannot be commonly used for high pin count devices due to limitations in PCB technology (via escape) and package warp. Vacuum soldering, which eliminates voids, will likely become more mainstream. Vacuum-assisted reflow soldering (vapor phase or modular reflow, which involves adding a vacuum zone) equipment currently costs 1.2 to 1.3 times more than more conventional equipment.

As equipment prices drop, vacuum soldering is likely to become more common. Other challenges in 2015 are not unlike those the electronics industry has faced over the past 10 years, but solutions will continue to require more advanced process technology and equipment. The result will be new processes, PCB and PCBA technology that would have been viewed as unachievable just a few years ago.



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