



**FARADFLEX**

**THE NEXT GENERATION OF  
BURIED CAPACITANCE™ MATERIAL**

**FARADFLEX™ BC24 · BC16 · BC12 · BC16T**

**OAK-MITSUI TECHNOLOGIES**

MITSUMI KINZOKU CORPORATE GROUP



MITSUMI  
KINZOKU

## INTRODUCTION

- Background of Buried Capacitance
- Performance Characteristics
- PWB Manufacturing Process
- Impedance Measurement
- Noise Measurement
- Conclusion





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# Background

## Current applications with Buried Capacitance

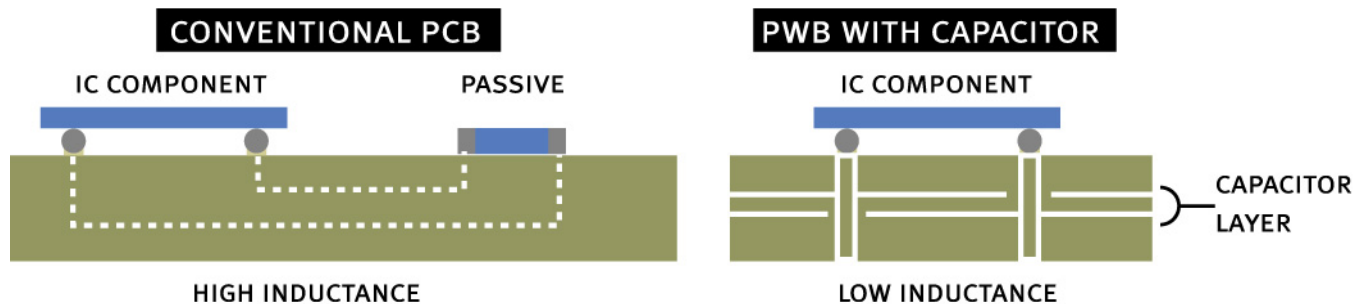
*Hi-end computers*

*Network servers*

*Network routers*



*Demand for power distribution system with low impedance*

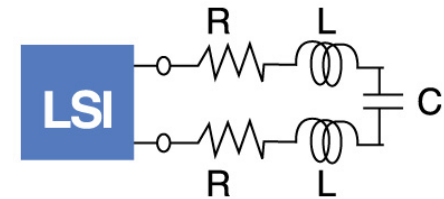
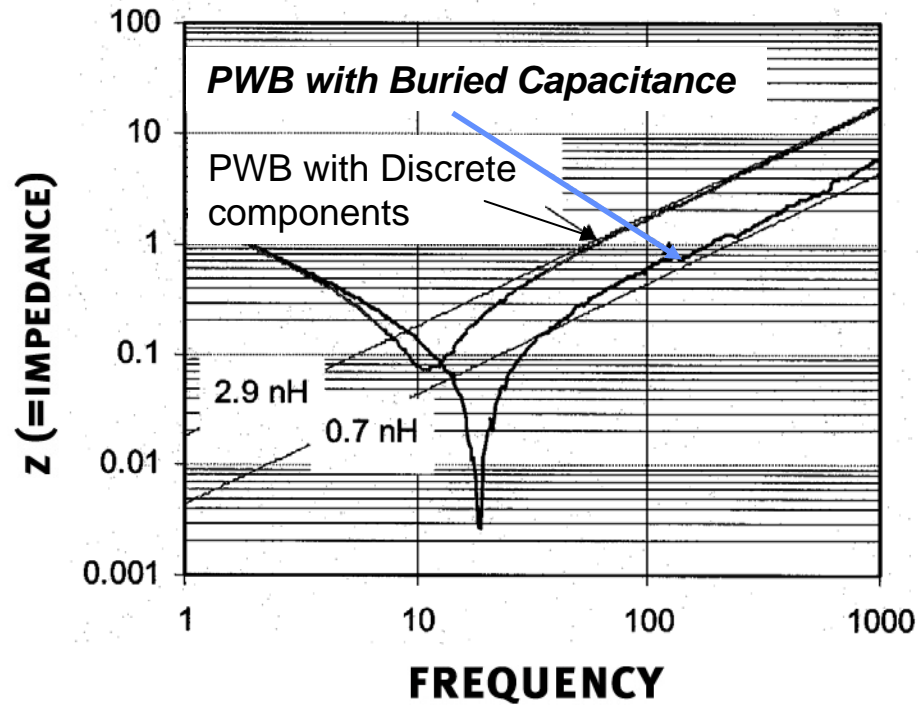




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# Background

## Lower Impedance compared to discrete components

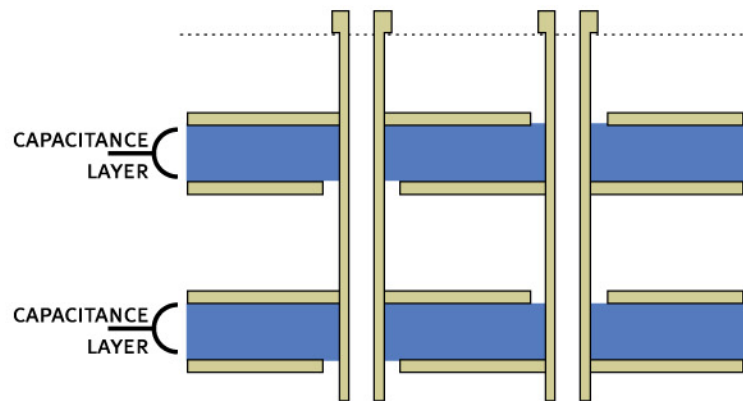




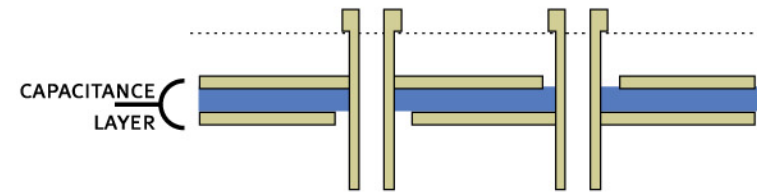
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# Background

## Demand for thin (<25micron) Buried Capacitance



**CONVENTIONAL MATERIAL**  
(55 μm)



**THIN CAPACITOR MATERIAL**  
**FARADFLEX™**

### Expectation by using Thin Capacitor Material

- Improvement in electrical performance
- Reduce cost
- Reduce thickness of the board





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# Product Data

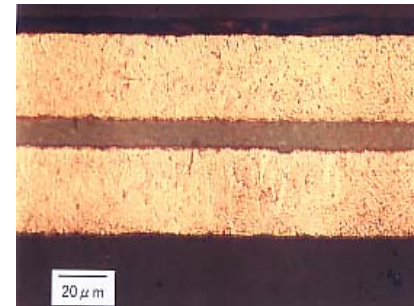
## Construction

**BC 12**



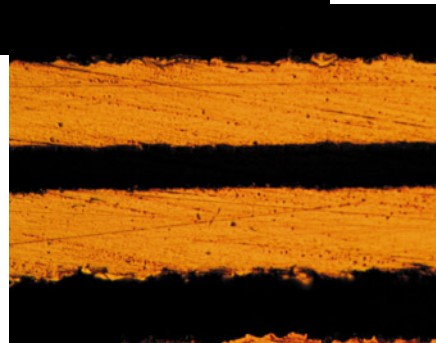
} 12 micron  
Polymer  
Dielectric

**BC 16T**



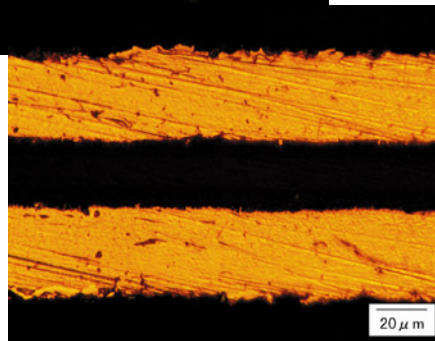
} 16 micron  
Polymer  
Dielectric  
with Hi-Dk  
Filler

**BC 16**



} 16 micron  
Polymer  
Dielectric

**BC 24**



} 24 micron  
Polymer  
Dielectric

\*Standard Copper thickness is 35micron

\*\*BC16T under development





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# Product Data

## Electrical Properties

Characteristics	Condition	Unit	<i>BC 24</i>	<i>BC 16</i>	<i>BC 12</i>	<i>BC 16T</i>
Capacitance	1GHz	pF/in	900	1500	2000	10,000
Dk	1GHz	N/A	4.6	4.6	4.6	25.0
Df	1GHz	N/A	0.012	0.012	0.012	0.014
Dielectric Thickness	Nominal	Micron Meter	24	16	12	16



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# Product Data

## Physical Properties

Characteristics	Condition	Unit	BC 24	BC 16	BC 12	BC 16T
Tg	DMA	Celsius	200	200	200	200
Peel Strength	As received	lb/in	>6.0	>6.0	>6.0	>4.0
Young's Modules	JIS 2318	GPa	4.8	5.8	7.2	TBD
Tensile Strength	JIS 2318	MPa	180	180	180	TBD
CTE	IPC TM650	PPM	30	30	30	TBD
Breakdown	1kV/sec	V	>5000	>4000	>4000	TBD
Insulation Reliability	85C/85%/35V	hr	>1000	>1000	>1000	TBD



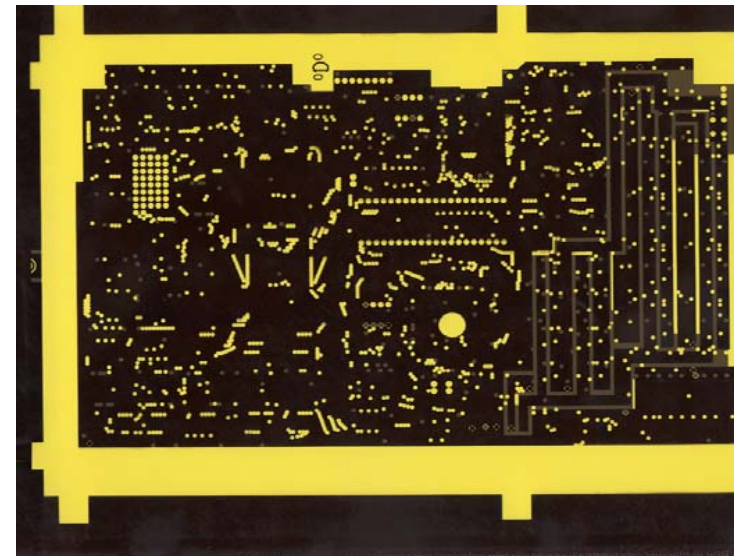
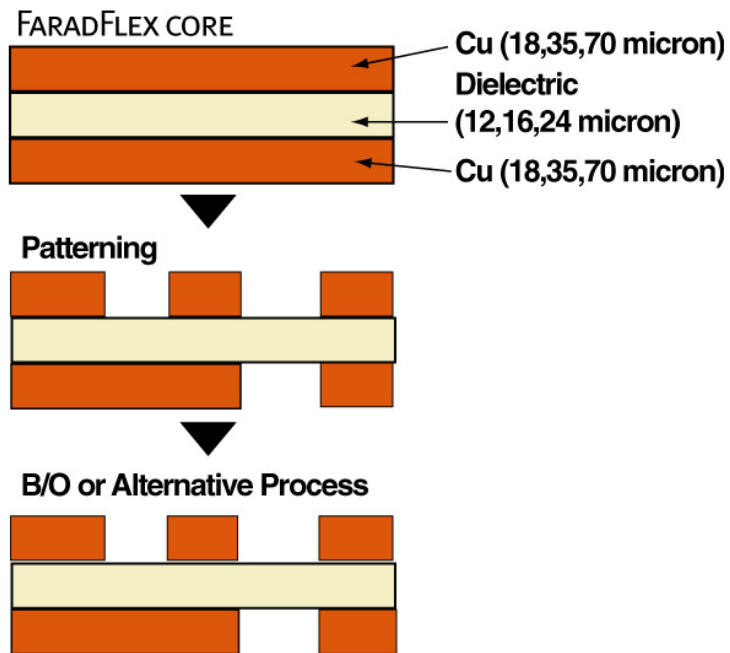




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# PWB Manufacturing Process

1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Dual sides)
5. Black Oxide or Alternative



B/O treated panel





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# PWB Manufacturing Process

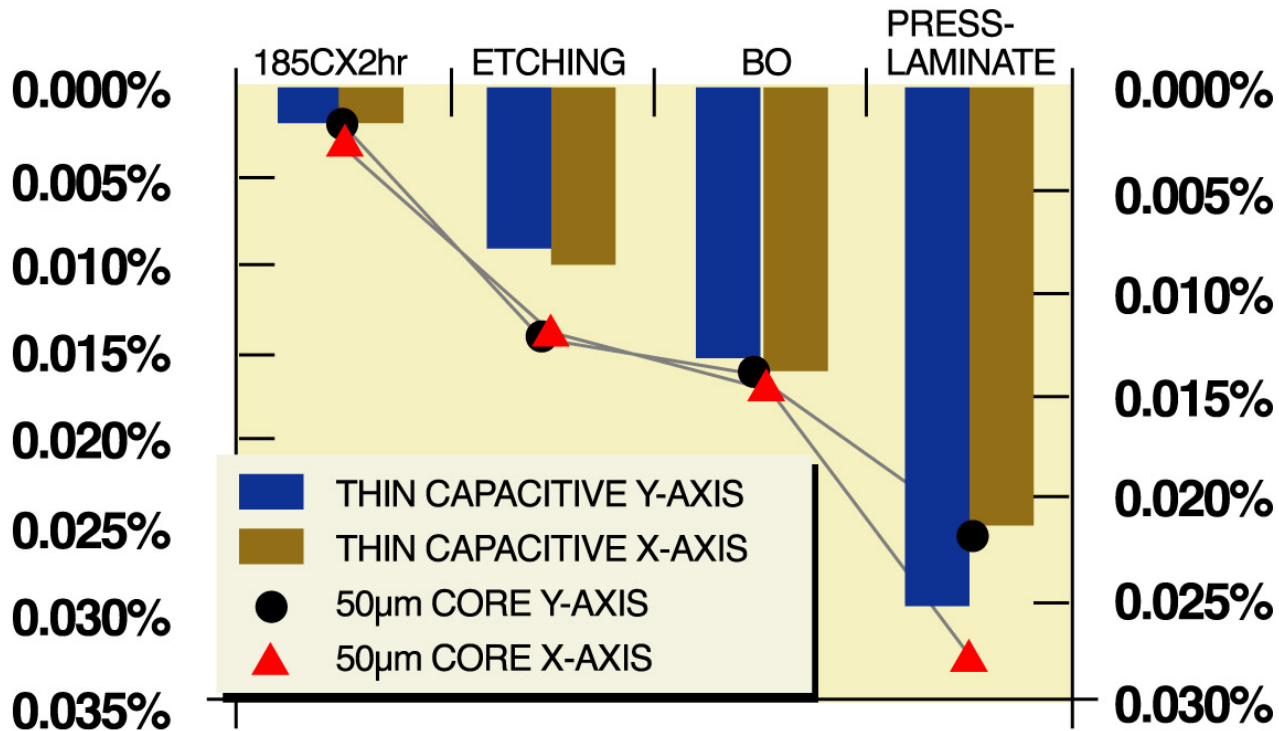
- Substrates Processed at Major PCB Facilities
- Standard I/L Processing
- Results
  1. **No loss** due to jams
  2. **No “blow out”** of Clearance holes
  3. **No separation** from border pattern
  4. **100 % Yield** at Hi-Pot (500 Volts)
  5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**



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# PWB Manufacturing Process

## DIMENSIONAL CHANGE: COMPATIBLE WITH FR-4 CORE



BC12 CAPACITOR





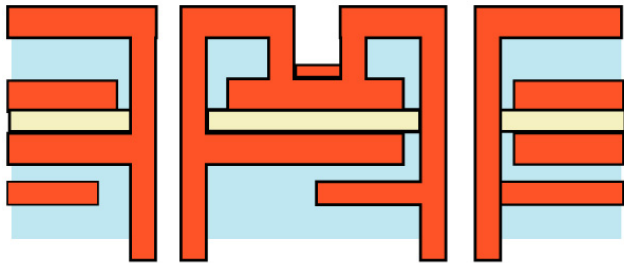
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# PWB Manufacturing Process

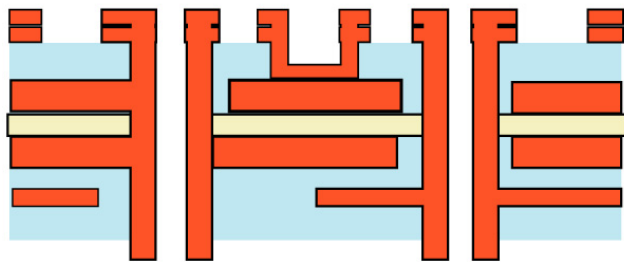
**B/O OR ALTERNATIVE PROCESS**



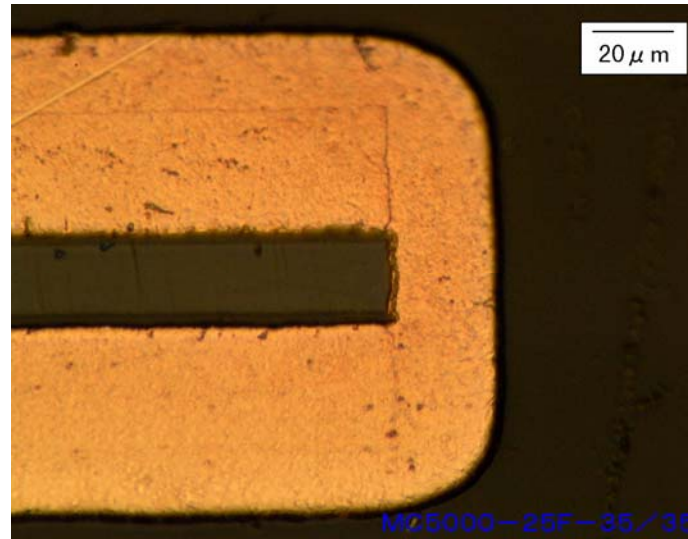
**THROUGH HOLE AND MICRO VIA FORMATION**



**PATTERNING**



After processing drilling, desmear and plating



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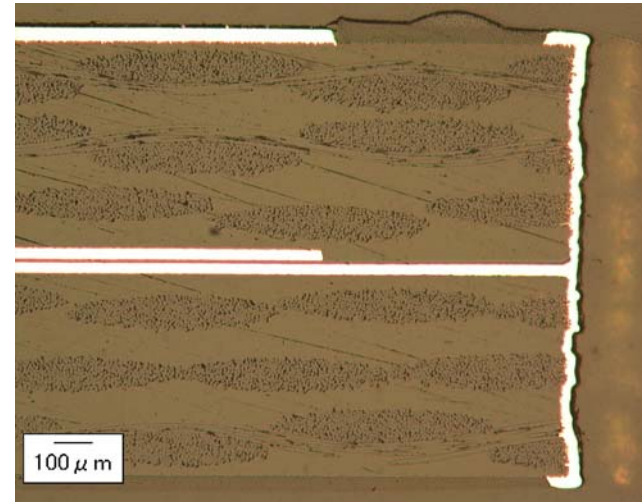
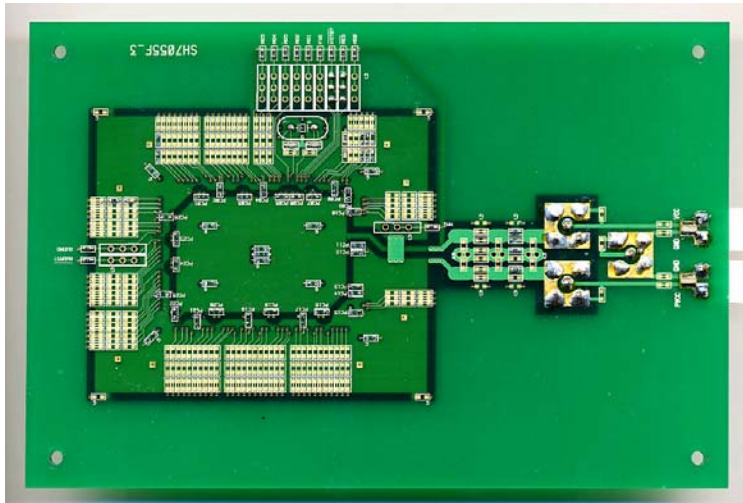




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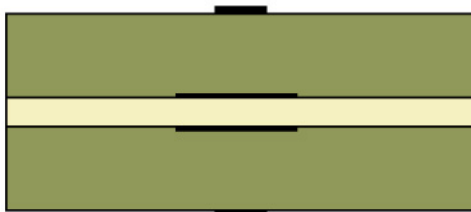
# PWB Examples 1

## 4 Layer Board



} **FARADFLEX**  
**BC12**

### 4 LAYER BOARD



L1  
L2 } FARADFLEX CORE  
L3 }  
L4

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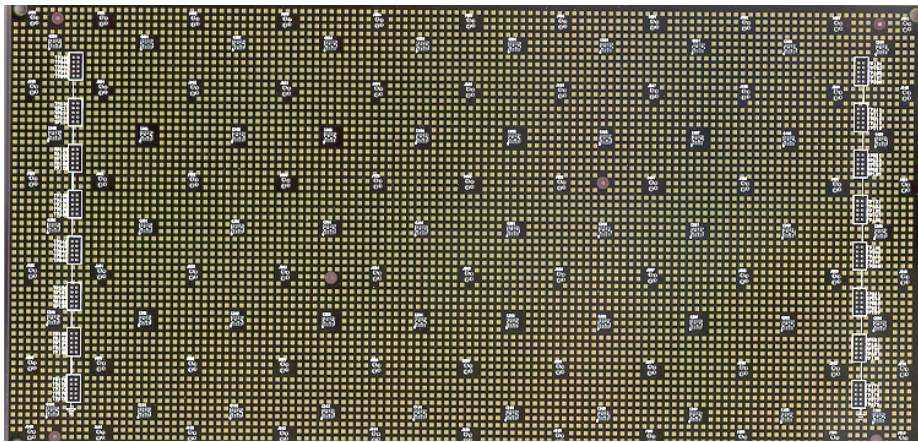




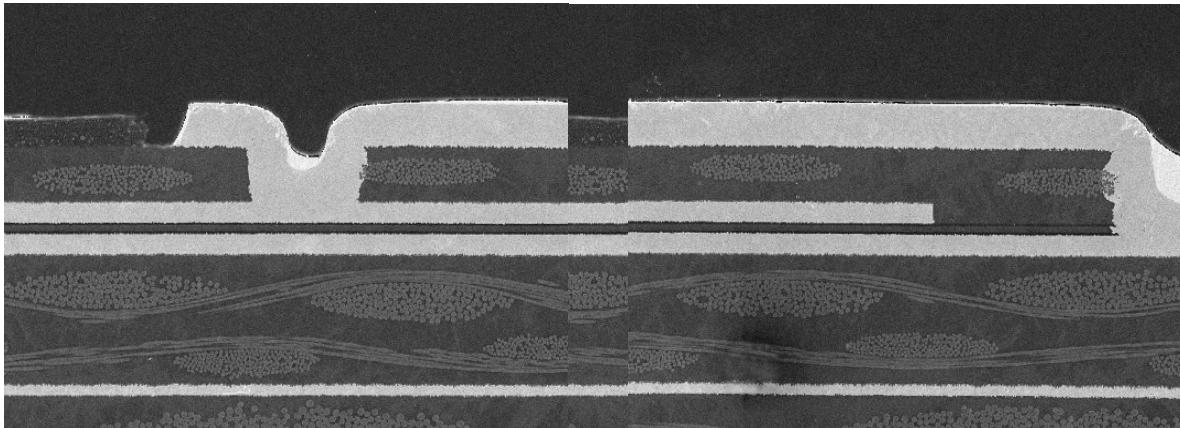
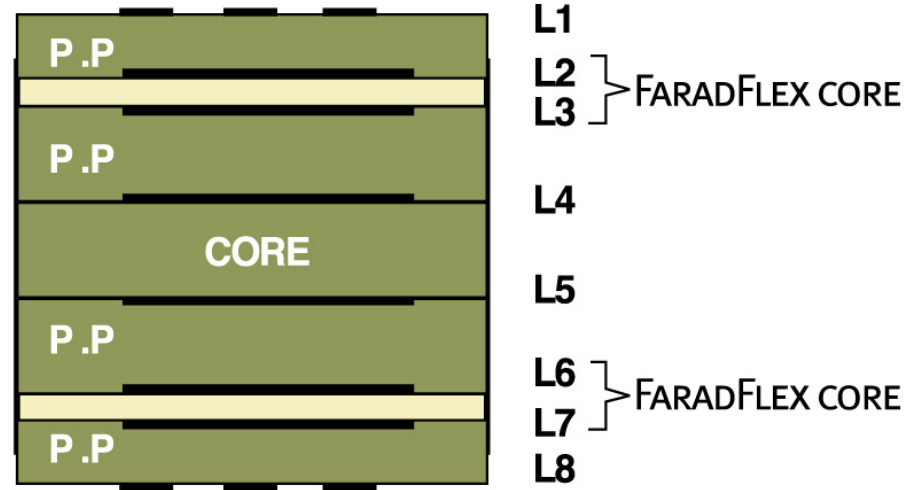
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# PWB Examples 2

## 8 Layer Board



## 8 LAYER BOARD with MICRO-VIA



FARADFLEX  
BC12

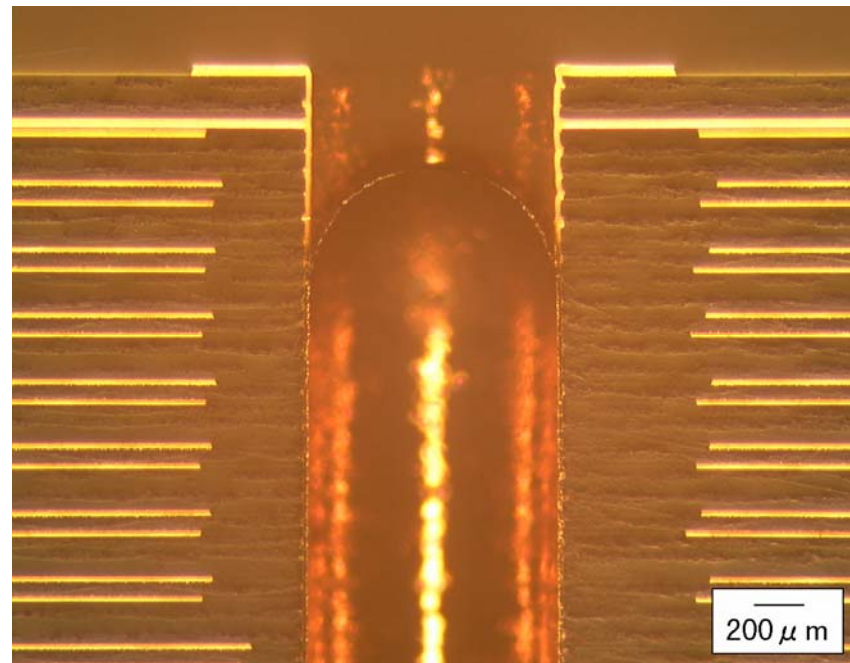
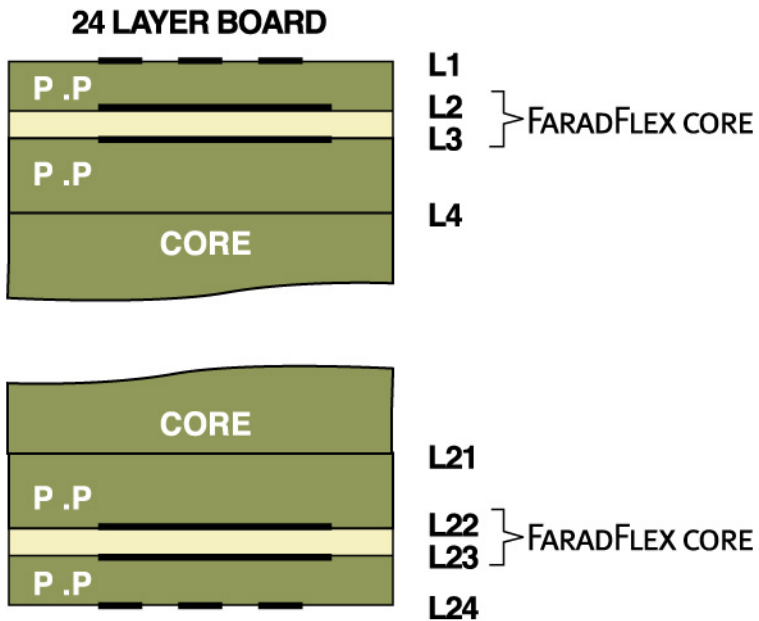




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# PWB Examples 3

## 24 Layer Board



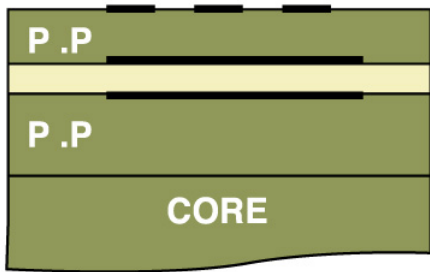
} FARADFLEX  
BC12



FARAD FLEX THE NEXT GENERATION OF BURIED CAPACITANCE™ MATERIAL

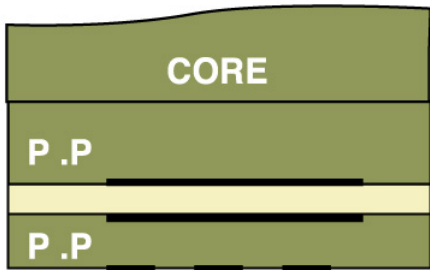
# PWB Examples 4

26 LAYER BOARD with MICRO-VIA



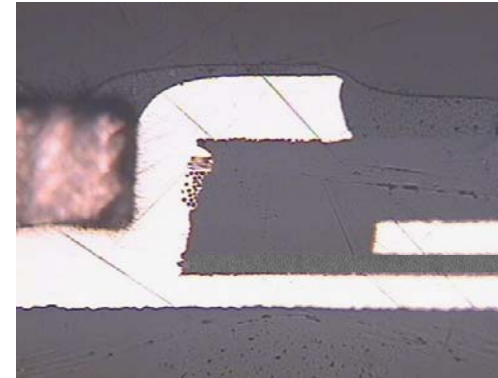
L1  
L2 } FARAD FLEX CORE  
L3

L4



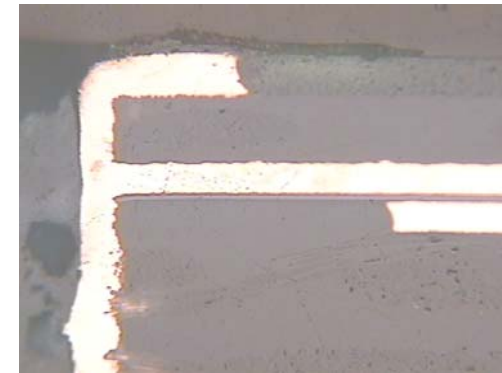
L23  
L24 } FARAD FLEX CORE  
L25  
L26

Micro-via Plating



FARAD FLEX BC24

Thermal Solder Shock 288C x6



FARAD FLEX BC12

## Reliability test

- Dielectric Withstanding Voltage : 500V Passed, No failure
- T-260 Time to Delamination : BC12 6.3min, BC24 5.2min
- Blind Via Plating Defects : No defects found
- Thermal Solder Shock – 6x : No defects found
- Liquid-Liquid : BC24 4.2%(500cycle)



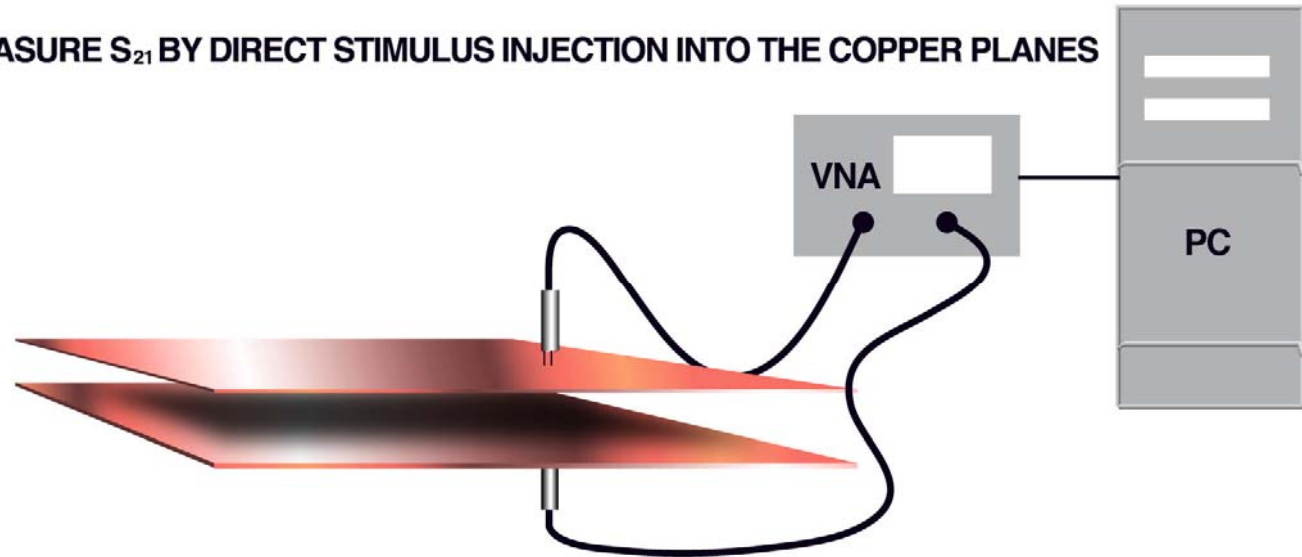




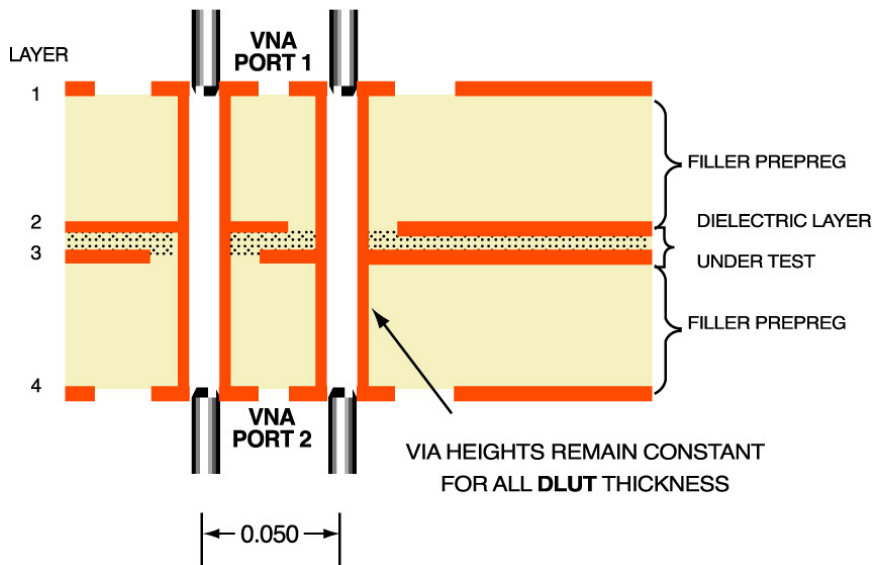
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# PWB Electrical Performance

MEASURE  $S_{21}$  BY DIRECT STIMULUS INJECTION INTO THE COPPER PLANES



## 4 LAYER TEST BOARD CROSS SECTION VIEW



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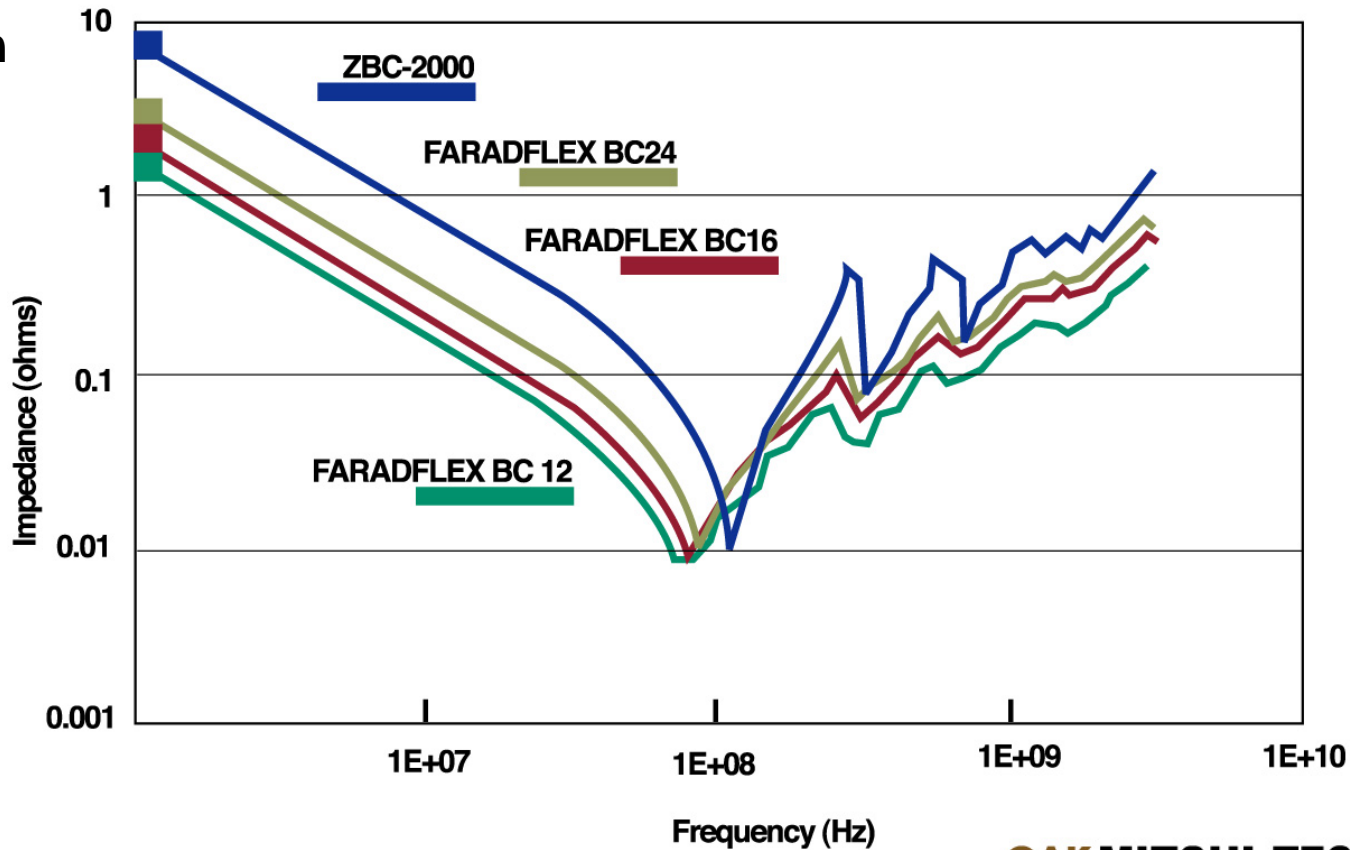


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# PWB Electrical Performance (Self Z)

## FULL SHEET RESONANCE SELF Z

Significant  
Reduction on  
Impedance



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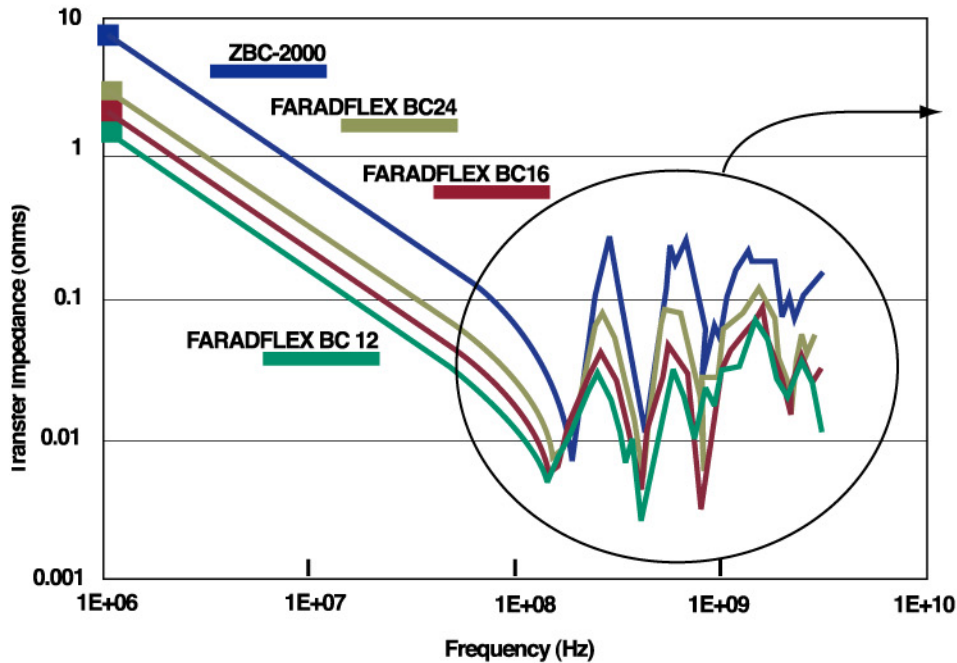


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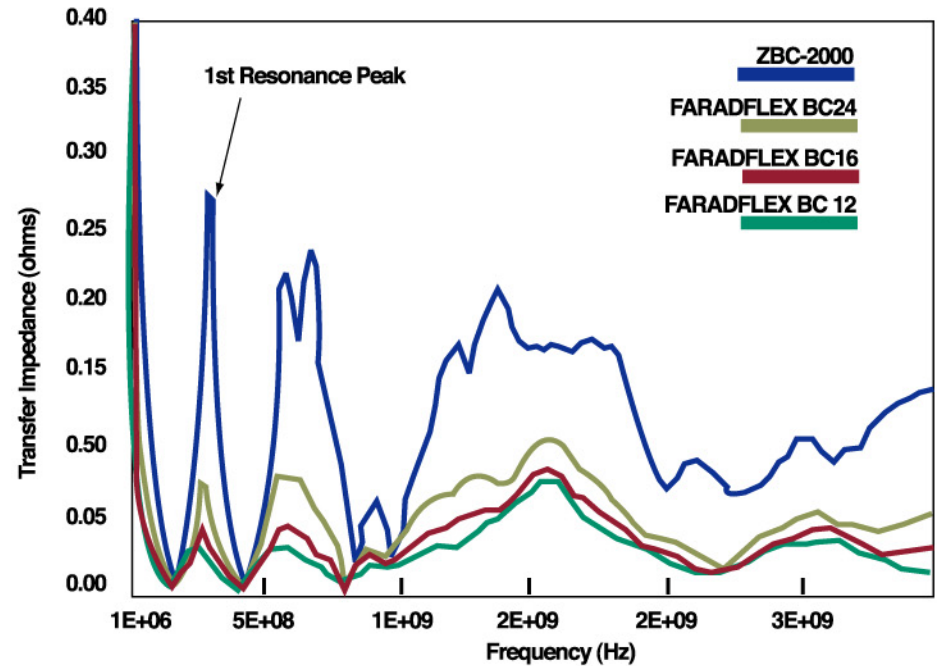
# PWB Electrical Performance (Transfer Z)

## Significant Reduction on Impedance

TRANSFER Z PROFILES AT 1" SEPARATION



TRANSFER Z HIGH FREQUENCY RESPONSE



Data Courtesy of Sanmina-SCI Corp.

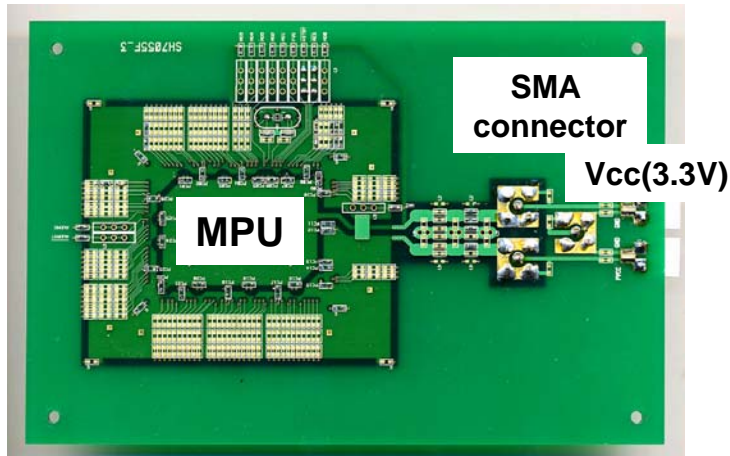




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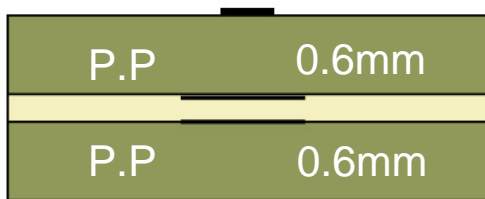
# PWB Electrical Performance (Transfer Z)

## Significant Reduction of EMI



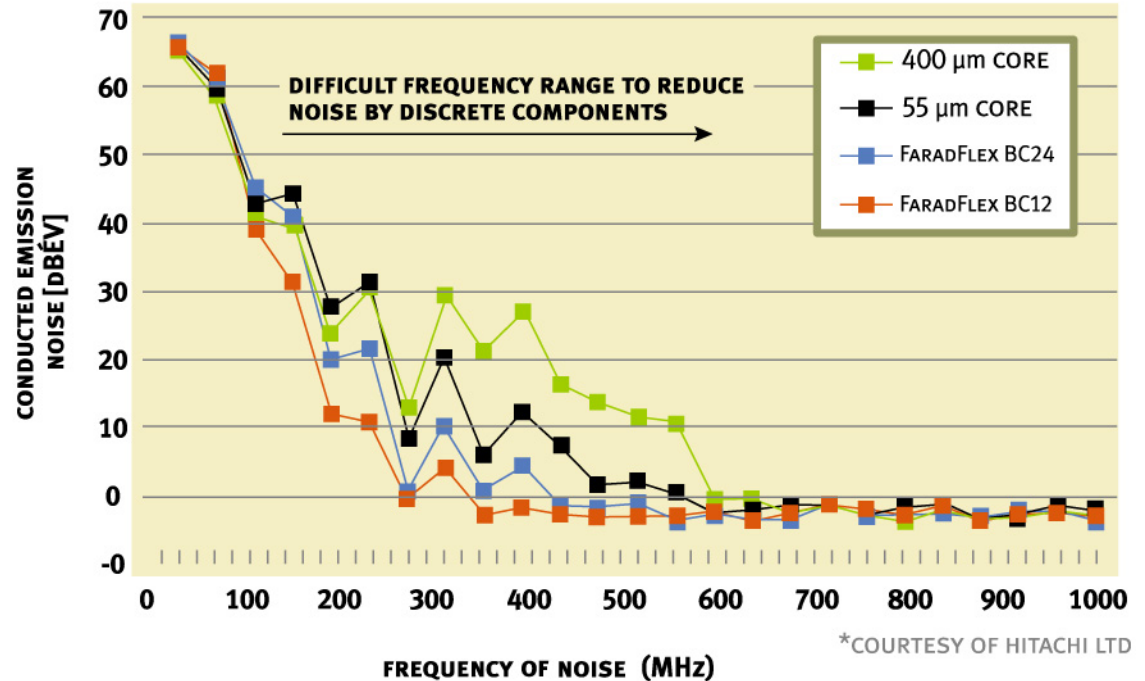
MPU (40MHz) is mounted on the other side of the board.

### 4 LAYER BOARD



L1  
L2 } FARADFLEX CORE  
L3 } AND CONVENTIONAL CORE  
L4

### SIGNIFICANT NOISE REDUCTION ON PWBS USING THIN CAPACITOR LAYER





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## Conclusion

- Thinner Materials for Buried Capacitance™ are required for improved Impedance Performance at high frequency
- Our New Substrate has *excellent* electrical performance and physical properties.
- It is *compatible* with PCB processing; a truly “drop in” material.

*The Product for High Speed Boards*

***FARADFLEX™***

***In Commercial Production!***

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THE NEXT GENERATION OF BURIED CAPACITANCE™ MATERIAL

# ***FARADFLEX™***

For more information contact:

John Andresakis

VP of Strategic Technology

(518) 686-8088

[john.andresakis@oakmitsui.com](mailto:john.andresakis@oakmitsui.com)

or visit us at [www.oakmitsui.com](http://www.oakmitsui.com)

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